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**Synthesising audible tones using
multiplexed light spectrum analysis**

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Executive Summary

This thesis presents the project development life cycle for synthesising audible tones using multiplexed light spectrum analysis. The project approach couples the analysis of visible spectrum light to create digitally synthesised audible tones. The project combines optoelectronic and communication systems to create a commercially viable prototype of a synaesthetic high quality digital electronic tone synthesiser with audio latency under 10ms. The project demonstrates the application of engineering principles in analysis, design, simulation, construction and evaluation, to produce a working prototype of a novel approach to generating sound through the discrimination of transmitted colour.

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Glossary

AC	Alternating Current
ADC	Analog-to-Digital Converter
CAD	Computer Aided Design
CLK	Digital Clock Signal
CRO	Cathode Ray Oscilloscope
DAC	Digital-to-Analog Converter
DC	Direct Current
DDS	Discrete Digital Synthesis
DSP	Digital Signal Processing
FPGA	Field Programmable Gate Array
GND	Signal Ground
IC	Integrated Circuit
IO	Input/Output
LED	Light Emitting Diode
MPSK	M -ary Phase Shift Keying
MSB	Most Significant Bit
MSPS	Mega Samples Per Second
NCO	Numerical Controlled Oscillator
opamp	Operational Amplifier
PCB	Printed Circuit Board
PSU	Power Supply Unit
QAM	Quadrature Amplitude Modulation
RAM	Random Access Memory
RGB	Red, Green, Blue
R_x	Receiver
RZ	Return-to-Zero
S3EDK	Spartan-3E Development Kit
T_x	Transmitter
VGA	Variable Gain Amplifier
VHDL	VHSIC Hardware Description Language
VSL	Visible Light Spectrum

Nomenclature

Ω	Resistance
φ_v	Luminous Intensity
λ_v	Spectral Wavelength
$V_\lambda(n)$	CIE Photopic Luminous Efficiency Function
Φ	Solid Angle
τ	Time Constant

1 Introduction

The aim of this project was to develop a device that generates audible tones from the analysis of transmitted visible spectrum light (VSL) through a finite open air communication distance. The transmitted visible spectrum light was the catalyst for deciding the frequency of the resultant audible tone. This project developed a working prototype combining optoelectronic, communication and digital signal processing (DSP) methodologies that produced a high quality digital electronic tone synthesiser with professional audio latency under 10ms [1]; providing a solid foundation for further commercial development.

The organisation of this chapter provides the rationale for developing a device to generate audible tones from the analysis of transmitted VSL through a finite open air communication distance. This chapter also presents the project objectives used as a benchmark for successful project completion and concludes by providing an overview of the organisation of this thesis.

1.1 Rationale

Creating musical tones with analog synthesisers is not a new concept, nor is making a digital equivalent, however, a synaesthetic component is added to a standard synthesiser when using VSL to create audible tones. The visual component to creating music (consisting of layers of tones) adds a further dynamic control to an artist's ability to paint a picture through sound. Recently, many researchers have created novel electronic music synthesis devices [2, 3, 4, 5, 6]. Their approaches have had successful results, however no commercial products have been developed from this academic research. This project provides a novel approach to generating an analog synthesiser, utilising recent advances in photodiode technology and combining multiple streams in electronic engineering.

As a multi-disciplinary project, the focus was to develop a communication system that used VSL as the primary method to characterise the resultant

tonal output of the synthesiser. As with all communication systems, the project consisted of a transmitter (T_x) and receiver (R_x) module; with user interaction only at the T_x and audio output at the R_x . By using VSL as the primary method to synthesise tones, it would be possible to further embed secondary data over the carrier wave of the VSL. As a benchmark for successful completion of the project, a set of project objectives were tabled to provide guidance during project development and to act as benchmark for successful completion. These objectives are discussed in the next section.

1.2 Project Objectives

In order to ascertain the successful completion of this project and guide decision making during development, two sets of project objectives were categorised: critical objectives and desirable objectives. Firstly, critical objectives were those that must be met under any circumstances in order to validate a successful project. Secondly, desirable objectives were considered extra goals for the project, but not critical to its success. Using the spiral management model [7], whereby the precedence of an outcome is affected by the circumstances that demand priority at a point in time, both project objective lists are unordered. The tabled list of critical and desirable project objectives are listed in Table 1 and Table 2 respectively.

Critical Objectives
Transmit VSL light from user input
Detect VSL light from a 50cm communication distance
Detect modulated VSL information
Create a synthesised tone based on the VSL spectrum
Have audible output via powered speakers or mixing desk
The system must have audio latency under 10ms

Table 1: Critical Project Objectives

1.3 Organisation

This thesis is organised in the following manner:

Desirable Objectives
Embed secondary user control data over VSL carrier wave Create controlled synthesised tones based on secondary user control data Increase the communication distance Decrease audio latency to under 5ms Add MIDI capability to the T_x and R_x Add balanced audio output to the R_x Create a user manual for the product

Table 2: Desirable Project Objectives

In Chapter 2, a feasibility report is presented outlining the necessary requirements pertaining to the plausible delivery of the critical project objectives. The chapter discusses initial experiments conducted in determining the transmission distance of various light sources and the spectral qualities of several different optical filters. The chapter also discusses the required amount of optical power that must be incident on the R_x module for colour information to be detected. The chapter concludes by presenting how ambient light could be decoupled from the R_x detection process, thus avoiding the corruption of colour information.

In Chapter 3, an analysis of the feasibility report is used to construct the project description and functionality. An analysis of the T_x and R_x module requirements (in terms of the critical and desirable project objectives), present a generic overview of the system, forming the basis of the project design.

In Chapter 4, the design proposal is presented. The chapter presents the individual components used to realise the implementation of the project, with respect to the controlling logic and firmware, the user interface, the required analog-to-digital and digital-to-analog conversion criteria, the colour information drivers and detectors, the audio output and presents the power requirements for the project.

In Chapter 5, the simulation results used to verify and corroborate the project design are presented. The simulations characterise the filter properties of the R_x using nodal voltage analysis and frequency response graphs. The firmware

simulations present the digital device timing diagrams simulated in VHDL, as well as the description of the logical constructs binding each module.

In Chapter 6, the construction of the project design is presented. The physical layout of the components and physical design considerations are discussed and detailed with respect to the T_x and R_x modules. The construction of the VSL transmitter and detector are discussed, as are thermal and external wiring considerations.

In Chapter 7, the results of evaluating each component described by the design and simulation chapters is presented. The chapter presents the system design and provides a modularised methodology to component and function testing. Problems encountered with the implementation of the project are discussed, as well as how these problems were overcome. The chapter concludes by presenting the evaluation of the entire system functionality.

In Chapter 8, we conclude the thesis by summarising the results of the project and show how it has met all critical project objectives. We also describe areas of future work for this project.

2 Feasibility

Based on the project objectives presented in Chapter 1, it was necessary to investigate the feasibility of using visible spectrum light (VSL) as a control mechanism in a communication system. The initial task for this project was to construct a set of experiments that would determine whether the project concept would be able to be realised through physical components. These early experiments formed the feasibility analysis for the transmitter (T_x) and receiver (R_x) modules.

This chapter describes each experiment, how they were conducted and the results that were obtained. The experiments were conducted to determine the distance that the transmitted VSL could travel and still be detected, the ability for the VSL detector to decouple ambient light from the transmitted VSL, and what type of filter would be required on the receiver to detect the VSL.

2.1 Transmission Distance

The first set of experiments were used to determine the distance that could be achieved under ideal and non-ideal conditions. Ideal conditions are under no ambient lighting, while non-ideal conditions are in broad daylight. The initial tests were conducted using several different types of widely available 5mm LED packages:

- Kingbright 5mm Full Color RGB Lamp
- 7,000mcd High Intensity 5mm Red LED
- 10,000mcd High Intensity 5mm Red LED
- 5,000mcd High Intensity 5mm Green LED
- 10,000mcd High Intensity 5mm Green LED
- 5,000mcd High Intensity 5mm Blue LED

- 10,000mcd High Intensity 5mm Blue LED

The light was detected using a TAOS TSL253R light-to-voltage sensor [8]. The TSL253R had a responsivity of 137mV at 635nm with a rise and fall time of 14 μ s. The TSL253R was a photodiode and amplifier in one package and did not have any selective wavelength properties, thus optical filters were required to be placed around the viewing window (see Figure 1) of each light-to-voltage converter. All of these tests used the TSL253R as the R_x .

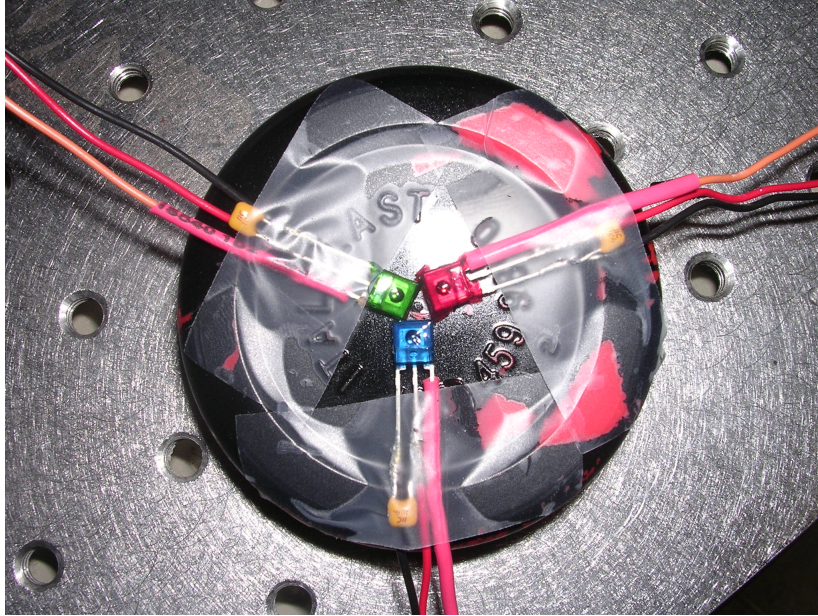


Figure 1: Closed System Photopic Detector Arrangement

A closed system test was devised to perform measurements under ideal conditions (see Figure 2). For this, a 42cm cylinder with a diameter of 60mm was used. End caps were placed at either end, with one end being the T_x while the other was the R_x . A 1kHz RZ pulse stimulated the T_x while a CRO was used to detect the output voltage from the R_x .

The tests comprised of determining the detectable voltage from each RGB LED with each corresponding RGB photodetector (the filtered TSL253R packages). These measurements were important for the recognition of discernable colours, the basis of this project. By being able to find a correlation

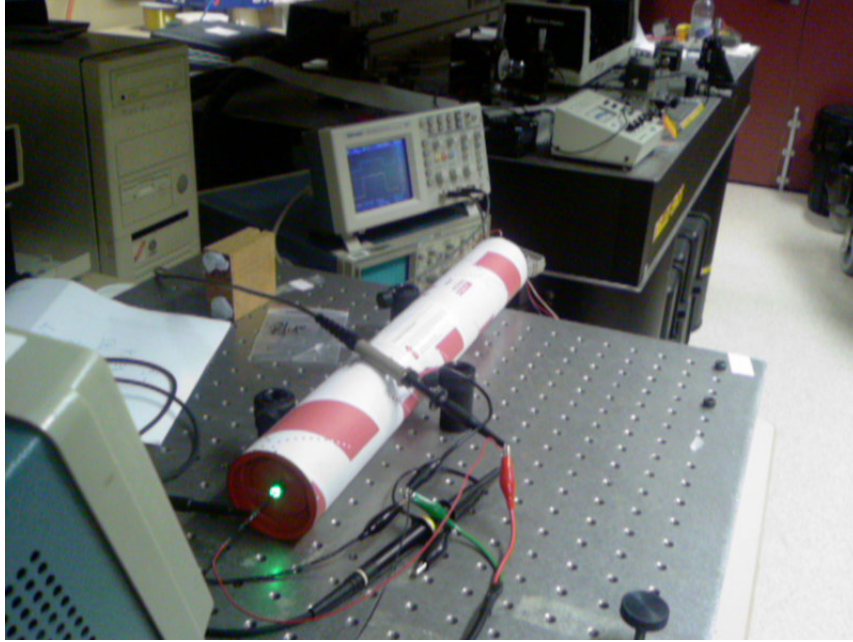


Figure 2: Closed System Overall Testing Setup

between the output voltage of the red LED with the red filter, the green LED with the green filter and the blue LED with the blue filter, it would be possible to translate this back into current ratios so that the range of differentiable colours could be determined. This test was also used to examine the ability of the RGB photodetectors to discriminate from which light source the final contributions were received.

Results of these tests are in Table 3 (for the 5mm RGB single package LED) and Table 4 (for the 5mm RGB individual package LEDs –7,000mcd Red; 5,000mcd Green; 5,000mcd Blue).

LEDs/Filters	Red	Green	Blue
Red	50mV	20.2mV	12mV
Green	6.2mV	8.8mV	7mV
Blue	13.4mV	14.8mV	58.4mV

Table 3: Closed System Testing: 5mm RGB Single LED – The diagonal voltages are not ideal.

LEDs/Filters	Red	Green	Blue
Red	3.60V	1.32V	1.34V
Green	154mV	1.48V	1.22V
Blue	608mV	1.17V	4.08V

Table 4: Closed System Testing: Individual 5mm RGB LED – The diagonal voltages are more suitable.

The closed system testing resulted in determining that individual high intensity LEDs are more suitable for this project than a single RGB LED package. The next experiment used three high intensity LEDs with the same luminous flux of 10,000mcd. The tests were conducted for the ideal and non-ideal case. The non-ideal experimental setup was similar to the closed system test, except the cylinder was removed so that the T_x and R_x were exposed to ambient light. The open system experiment was performed under ‘Cool White’ coloured fluorescent tubes to simulate broad daylight.

The result of these experiments are shown in Table 5 (for the ideal case) and Table 6 (for the non-ideal case).

LEDs/Filters	Red	Green	Blue
Red	4.16V	1.84V	800mV
Green	90mv	1.3V	960mV
Blue	224mV	500mV	1.62V

Table 5: Closed System Testing: Individual 10,000mcd 5mm RGB LED – The diagonal voltages show signs of respectable ratios that can be differentiated.

LEDs/Filters	Red	Green	Blue
Red	3.52V	2.16V	1.4V
Green	96mV	1.08V	1.2V
Blue	184mV	400mV	1.06V

Table 6: Open System Testing: Individual 10,000mcd 5mm RGB LED – The diagonal voltages show a discernable drop in differentiable voltages and are compromised by the red LED.

The results obtained from the open and closed system testing of the individual 10,000mcd 5mm RGB LEDs was that under non-ideal conditions, the red LED was dominant. This result was attributed to the RGB photodetectors

being susceptible to ambient light, as the package had no way of filtering this other than with the optical filters.

2.2 Determining Filter Types

The ‘optical filters’ used in the previous experiments were regular sheets of coloured cellophane. Although not an ideal medium to use for filtering because their spectral characteristics could not easily be matched to the LEDs; however, they were a cheap alternative to expensive selective optical wavelength filters. Other combinations of cellophane and coloured sources were used to better approximate the spectral response of the LEDs, these were: blue/purple cellophane, purple cellophane, yellow/green cellophane, lemon mint Tic-Tac packaging (greenish colouring)/green cellophane, extra strong mint Tic-Tac packaging (bluish colouring)/blue cellophane. The results of these experiments are omitted for brevity, however the analysis of these results was that better filtering would be required for the RGB photodetector or a different choice of photodetector.

As the TSL253R light-to-voltage converter could not decouple the DC (ambient) light, an alternative photodiode arrangement was examined. The EPIGAP selective photodiode range was chosen for its inherent ability to filter optical wavelengths due to the technology used to construct the photodiode. These are narrow bandwidth, high spectral sensitive devices for red, green and blue visible wavelength ranges. Using these photodiodes it would also be possible to bypass the DC component by incorporating a filter into the pre-amplifier stage of the R_x .

The spectral responses for the green and blue EPIGAP selective photodiodes are shown in Figure 3 (for the green selective photodiode) and Figure 4 (for the blue selective photodiode). Professional camera filters from LEE Filters were obtained in the event that cross-over occurs between the green and blue LEDs for the blue selective photodiode.

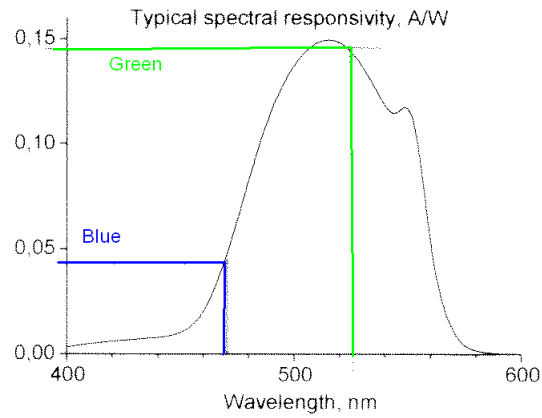


Figure 3: EPD-525-0-1.4 Spectral Response – Relative spectral responsivity for green and blue wavelengths of the selected LEDs

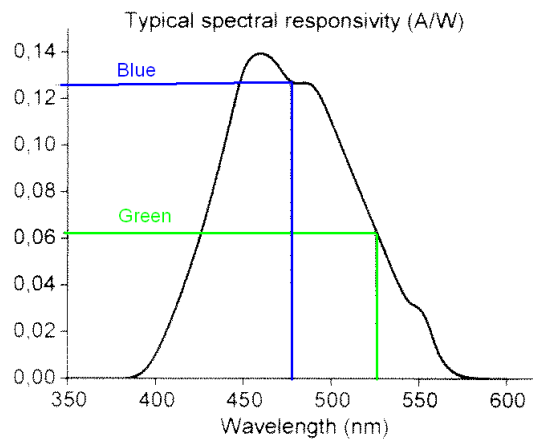


Figure 4: EPD-470-0-1.4 Spectral Response – Relative spectral responsivity for green and blue wavelengths of the selected LEDs

2.3 Determining Optical Power

Having determined that the project will use the EPIGAP selective photodiodes, a hypothesis of the quantity of high intensity 10,000mcd RGB LEDs required for the project was made. To make this hypothesis, a series of calculations based on the data available for each RGB LED and RGB photodiode was used in conjunction with radiometric and photometric equations.

The LED datasheets provide the viewing angle, θ , spectral wavelength range, λ_v , and luminous intensity, φ_v . These values in conjunction with the CIE Photopic Luminous Efficiency Function, $V_\lambda(n)$, can be used to find the radiant intensity for each RGB LED in watts per steradian.

$$\varphi_v = 683 \cdot \varphi \cdot \int_{\lambda_v} V_\lambda(n) d\lambda$$

$$\varphi = \frac{\varphi_v}{683 \cdot \int_{\lambda_v} V_\lambda(n) d\lambda}$$
(1)

The results of the above calculations are in Table 7 [9].

LED	Spectral Range (λ_v)	Radiant Intensity (φ)
Red	605nm – 645nm	0.484636 W sr ⁻¹
Green	505nm – 545nm	0.19148 W sr ⁻¹
Blue	445nm – 495nm	1.99068 W sr ⁻¹

Table 7: Radiant Intensity Calculations for each of the high intensity 10,000mcd RGB LEDs

Using these results, the radiance was calculate, ie, the power per unit solid angle per unit projected source area (see Figure 5).

$$L = \frac{\varphi}{\Phi \cdot dA \cdot \cos(\Theta)}$$
(2)

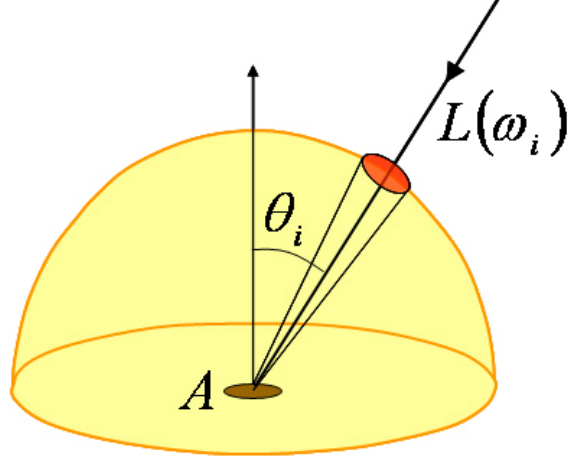


Figure 5: The effect of Radiance, $L(\omega_i)$, on a projected solid area, A , with respect to the solid angle, θ_i .

In these radiance calculations, Φ , the solid angle, was evaluated as $\Phi = A/r^2$, with $A = 1$ and $r = 1$, as the projected source area was a 1m^2 square surface. Θ was calculated with respect to the half viewing angle of the LEDs, thus $\Theta = \theta/2$. This reduced Equation 2 to:

$$\begin{aligned}
 L &= \frac{\varphi}{\Phi \cdot dA \cdot \cos(\Theta)} \\
 &= \frac{\varphi}{\Phi_{(L \times W)} \cdot \cos(\theta/2)} \\
 &= \frac{\varphi \cdot r^2}{A \cdot \cos(\theta/2)} \\
 \therefore L &= \frac{\varphi}{\cos(\theta/2)}
 \end{aligned} \tag{3}$$

LED	Radiance ($\text{W sr}^{-1} \text{ m}^2$)
Red	0.484636
Green	0.193133
Blue	2.021389

Table 8: Radiance Calculations for each of the high intensity 10,000mcd RGB LEDs.

The results in Table 8 were used with the available data for the active area and responsivity of the photodiodes to establish a relationship between each RGB LED and its corresponding RGB photodiode. These calculations are summarised in Table 9.

LED	LED L	L Photodiode	Photodiode Responsivity
Red	484nW mm ⁻²	62.92nW	26.42nA
Green	193nW mm ⁻²	231.6nW	57.9nA
Blue	2021nW mm ⁻²	2425.2nW	727nA

Table 9: RGB LED Radiance acting on its corresponding RGB photodiode.

The results from Table 9 allow a hypothesis to be formed based on the radiance from one RGB LED acting on its corresponding RGB photodiode at 1m. These results are summarised in Table 10, Table 11 and Table 12.

LED	Response from Photodiode	Number of LEDs for response
Red	420 μ A	15,897
Green	250 μ A	4,317
Blue	300 μ A	412

Table 10: How many LEDs? - A: Results for 1/1000th of the maximum RGB photodiode response.

LED	Response from Photodiode	Number of LEDs for response
Red	100 μ A	3,785
Green	100 μ A	1,727
Blue	100 μ A	137

Table 11: How many LEDs? - B: Results for 100 μ A RGB photodiode response.

LED	Response from Photodiode	Number of LEDs for response
Red	1 μ A	37
Green	1 μ A	17
Blue	1 μ A	2

Table 12: How many LEDs? - C: Results for 1 μ A RGB photodiode response.

From determining the number of LEDs required for different current responses from the RGB photodiodes, a 1 μ A response can be achieved from

using 37 red, 17 green and 2 blue high intensity 10,000mcd LEDs. These calculations assumed an even distribution of the radiance is achieved from the LEDs onto the surface at a distance of 1m. To account for these discrepancies, 40 red, 20 green and 6 blue LEDs are chosen as the quantity required for this project. Testing of this numerical approximation will occur once the hardware is built.

2.4 Decoupling Ambient Light

The closed and open system experiments determined that the TSL253R was not capable of decoupling ambient light from its resultant output. The reasoning for this can be shown in Figure 6. It is evident that the TSL253R light-to-voltage converter insufficiently handles ambient lighting as a result of having an internal transresistance amplifier. The $16\text{M}\Omega$ feedback resistor with the internal capacitance increases the τ of the system, thus affecting the overall system bandwidth.

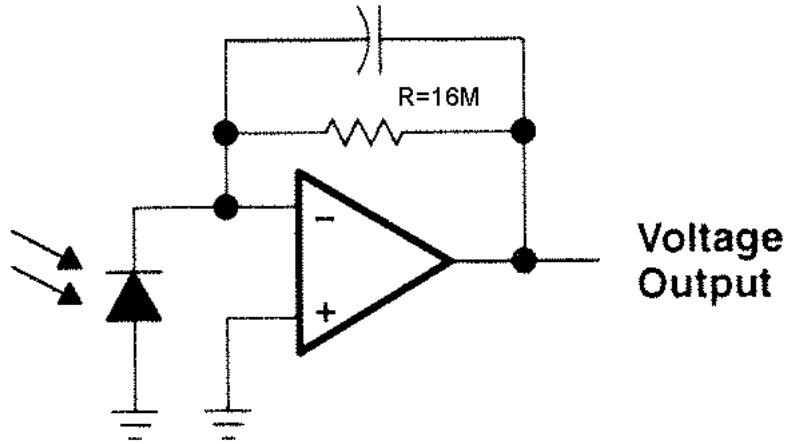


Figure 6: TSL253R Internal Block Diagram – The total rise and fall time of this device was $14\mu\text{s}$

With the selection the the EPIGAP selective photodiodes, an AC coupled amplifier can be used to filter out the DC component of light. The AC component conforms to having a modulation technique that will allow amplitude and data to be transmitted across the communication channel irrespective of DC conditions.

2.5 Summary

This chapter presented the results from the feasibility study used to establish the viability of this project's objectives as described in Chapter 1. The feasibility study conclusively showed that it would be possible to fulfill the project's critical objectives.

As a result of these feasibility findings, the project's two modules may be examined at a greater level of detail. This is presented in the next chapter.

3 Analysis

The previous chapter presented the feasibility report on the viability of generating audible tones from the analysis of transmitted visible spectrum light (VSL) through a finite open air communication distance. The feasibility report showed that it would be possible to use VSL as the primary data sent in a communication system.

This chapter presents an analysis of the transmitter and receiver modules that comprise the framework for this project. This chapter first analyses the requirements of the transmitter, followed by the receiver.

3.1 Transmitter Analysis

The transmitter (T_x) module is responsible for user interaction and transmission of the resultant VSL for the light synthesiser. User interaction is in the form of seven keys, one rocker switch and three control knobs. The rocker switch provides the user with the ability to switch octaves on the synthesiser, while the control knobs affect the attack, sustain and decay of the synthesised audio waveform. The seven keys represent the seven musical notes: A, B, C, D, E, F and G. The pairing of frequencies of sound and those of light have been well documented [10].

This module will attempt to use the optical power of RGB LEDs (see Figure 7) as triggers for producing audible tones at the receiver module. To achieve this, the ratio of RGB LED intensities will vary for each frequency trigger, thus proposed colour information for each tone must be tested with the selected LEDs in order to confirm that the range is acceptable. Alternative tone and colour mappings may be investigated if the initial colour do not allow for distinct discrimination at the receiver.

Synthesisers use envelope shapers that control the synthesised audio output. This module will also consist of an octave shifter and three control knobs that allow for the sustain, attack and delay and pitch of the resultant tone to be altered. A desirable objective is to use this extra tone control as

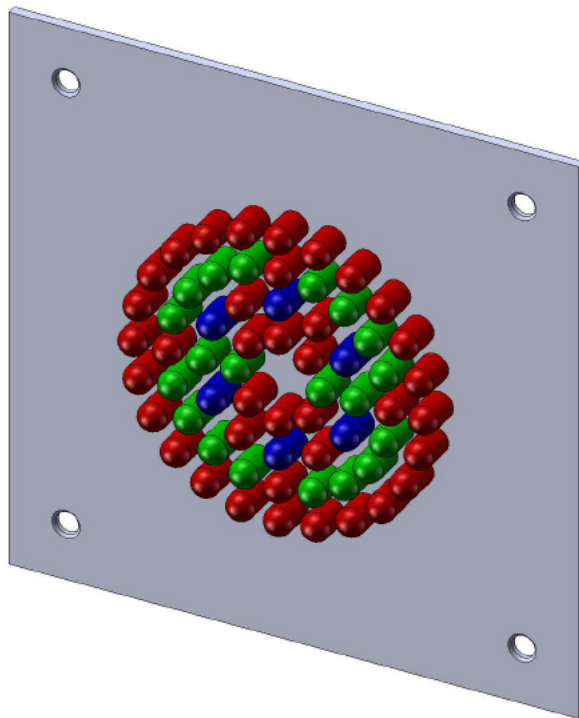


Figure 7: T_x LED Transmitting Module.

embedded data within the main colour information transmitted across the communication channel. As data other than colour is being sent across the communication channel, a modulation technique will need to be considered for transmission. The exact modulation technique must be investigated taking into account that light should always be visible from the module and that the data sent will be asynchronous. The effect of ambient light could also impact on the transmitted colour information and the modulation technique, thus adding the criteria that the modulation method work under AC conditions.

3.2 Receiver Analysis

The receiver (R_x) module is responsible for detecting and decoding the colour information sent across the open air communication channel from the transmitter. The critical objective is to discriminate the transmitted colours from a minimum distance of 50cm, a desirable objective is to enable detection at distances greater than 50cm. The receiver detects the incoming stream using photopic detectors for each RGB colour component. The received colour information is decoded so that processing can determine the resultant tone to be produced. If secondary data is embedded in the colour information, the data stream must be decoded so that it may be used to alter the resultant tone.

The photopic detectors will need to be considered with respect to the modulation technique that will be investigated. The detectors will need to be able to discriminate the colour information sent for each frequency and be immune to the effects of ambient light on the colour information detected. When the colour information is successfully processed, a direct digital synthesis of an audible tone related to the colour information transmitted is produced. If secondary data is embedded in the colour information, it is used in conjunction with the synthesis process to alter the resultant audible tone. The audible tone is then converted to an analog signal that is output

via stereo RCA sockets can be used directly by powered speakers or a mixing desk to produce the final audible tone.

3.3 Summary

In this chapter, the functionality of the individual project modules was presented. The analysis of the T_x module specified that the colour information was stimulated by user input, while the R_x module generated audible tone output as a result of a specific mapping of colour to frequency. Desirable outcomes for embedding secondary user controlled data to modify the resultant tone was discussed, as well as the criteria for decoupling ambient light from impacting on the colour information transmitted and detected.

In the next chapter, this project analysis is discussed in terms of physical components and requirements for fulfilling the critical functionality described in this chapter, while also presenting the foundation for desirable project outcomes.

4 Design

In the previous chapter, the functionality of the individual project modules was presented. The analysis of the T_x module specified that RGB LED colour was used to engage the R_x module to generate different audible tones as a result of a specific mapping of colour information to frequency.

In this chapter, a design solution for the project is presented based on the project analysis and feasibility report in the previous chapters. We present a systematic approach to the development of a physical prototype of synthesiser capable of producing audible tones from the discrimination of colour information sent across an open air communication channel.

4.1 Logic Controller

The main logic controller was chosen to be a Field Programmable Gate Array (FPGA). This choice was based on the parallel requirements of both the transmitter and receiver modules. The selected FPGA needed to fulfill the following requirements:

- Contain a large amount of configurable logic cells;
- Have a large amount of input and output ports available;
- Large amounts of block RAM available; and
- Clock managers to ensure internal clocking signal integrity.

These requirements were fulfilled by the Xilinx Spartan-3E FPGA Family of devices [11]. Rather than obtaining an individual FPGA and having a multi-layered circuit board made for this project, a Spartan-3E development kit (S3EDK) was to be used for this project [12]. The key features of the S3EDK fulfilled the requirements set out above. The development kit is shipped with an XC3S500E Spartan-3E with over 10000 logic cells, 360kB of addressable block RAM and four digital clock managers. The development

kit had a total of forty input/output (IO) ports available; thirty-five bi-directional IO ports, and five dedicated input ports. These IO lines were accessible via the J3 expansion header, and the physical inter-connection between the developed modules and the S3EDK required an FX2 Hirose receptacle connector [13].

A connector board was created for communication between the S3EDK and the individual T_x and R_x modules [14, 15]. The connector board mapped the IO lines of the J3 expansion header to a 50-Way IDC header, with the T_x and R_x modules attached to the connector board via a length of ribbon cable [16, 17, 18]. As there are two modules, individual connector boards were made for each, and the project required two S3EDKs.

4.2 User Interface

As described in Chapter 3, the primary user interface is situated on the T_x module. The primary user interface on the T_x dictates the resultant colour combination sent over the communication channel in the form of push buttons. The user interface on the T_x also provides functionality for octave shifting via a momentary rocker switch, and control knobs for waveform shaping. The R_x module does not have a user interface, but it provides an expansion header in the form of a 10-Way IDC header that has the capability to accept five user inputs [17]; a feature for future development.

4.2.1 Keys

Many modern synthesisers use a piano styled keyboard as user input, and this design could easily be etched into copper (see Figure 8). Unlike modern synthesisers, this project's aim was to control the resultant frequency as a result of user key presses, it was not concerned with controlling the amplitude of the resultant tone by measuring the velocity of each key press. To conserve board space and reduce manufacturability issues, it was decided that this project would use seven momentary push buttons to trigger the resultant frequency. The significance of the seven push buttons was based on the

seven major notes of a typical piano keyboard (A, B, C, D, E, F and G), with sharps omitted (B[#], C[#], D[#], F[#] and G[#]).

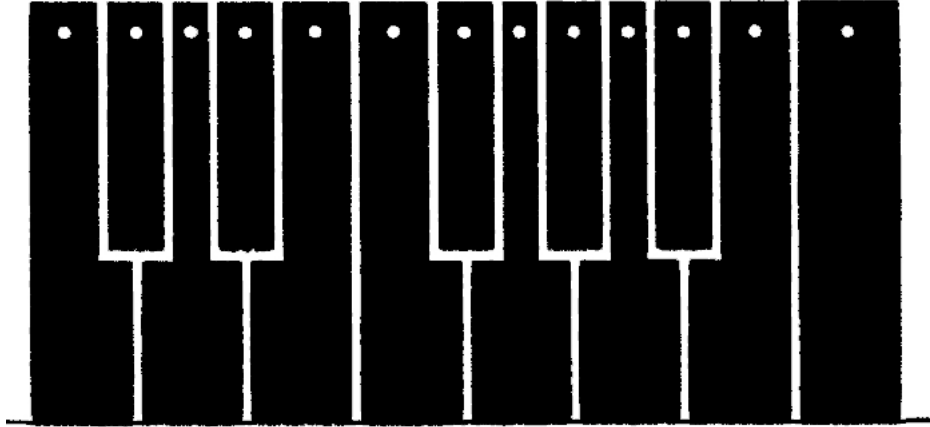


Figure 8: Piano Keyboard PCB Layout [19]:

The electrical design of the push button circuitry (see Figure 9) was designed so that when pressed, the FPGA would recognise a logic high [20]. Although the button debouncing will be primarily controlled by the FPGA, the 10nF capacitor in Figure 9 provides some form of electrical debouncing. Each of the push buttons connect to separate input ports on the S3EDK.

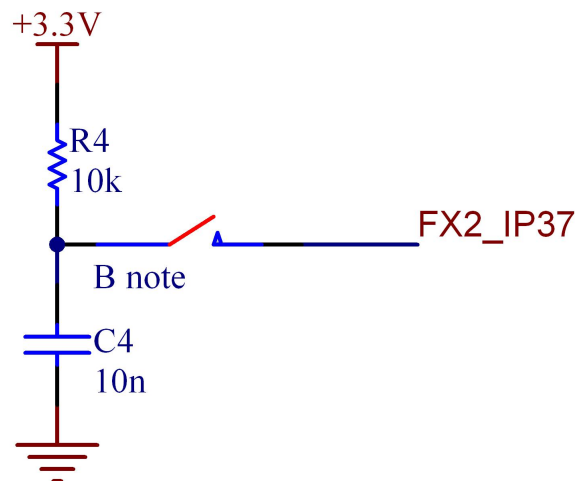


Figure 9: Push Button Circuit

4.2.2 Octave Shifter

In addition to sending frequency triggers through colour information, a desirable objective of this project was to embed secondary user control data in the transmission. This secondary data would contain the transmission of octave shifts, allowing the receiver to scale up and down frequency values in each octave typical of a modern synthesiser with piano styled keyboard input.

The electrical design of the momentary rocker switch (see Figure 10) was designed so that when the user pushes either up or down on the lever, a logic high pulse was sent to the FPGA [20]. As with the push buttons, the FPGA will control the switch debouncing, and the 10nF capacitor in Figure 10 serves to provide some form of electrical debouncing for the switch. The two outputs of the switch are sent to two separate input ports on the S3EDK.

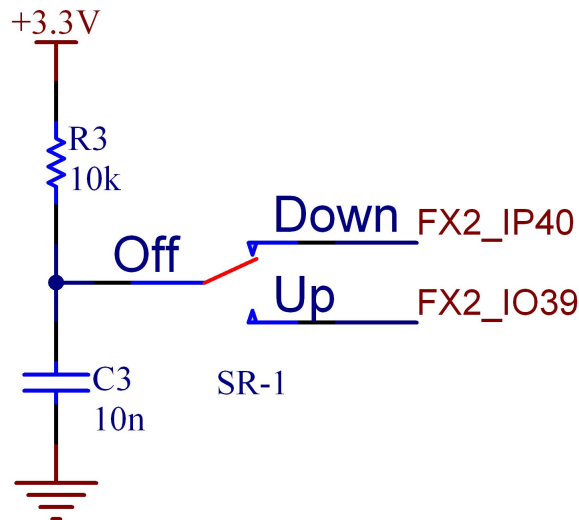


Figure 10: Rocker Switch Circuit

4.2.3 Control Knobs

As discussed in the previous section, embedding additional data with the transmission of colour information was a desirable project objective. Three

control knobs used to shape the resultant tonal frequency produced by R_x are included in the T_x design. These control knobs control the attack, sustain and decay of the resultant tone that was produced.

The three control knobs used for waveform shaping consist of three $1k\Omega$ linear potentiometers, with each wiper connected to a separate channel of the T_x module's ADC [21]. The A and B terminals are connected to +3.3V and GND respectively.

4.2.4 Embedding Secondary Data

The transmission of embedded secondary user control data required a technique that could co-exist with the AC coupled transmission of the colour information used to generate the desired tonal frequency. A suitable solution was to use a modulation technique that would not degrade the ability for colour to be used as the primary transmission format.

The project design considered M -ary phase shift keying (MPSK) or quadrature amplitude modulation (QAM) as viable options. One problem with MPSK was that the receiver might not be able to distinguish small differences in phase, thus limiting the bit rate of the transmission. QAM offered a lower susceptibility to noise and an increased bit rate compared to that of PSK. The minimum bandwidth required for MPSK or QAM is [22, 23]:

$$f_c \pm N_{\text{baud}}/2 \quad (4)$$

The colour detection design was required to take Equation 4 into account when designing the filter cut-off frequencies (see Figure 11).

4.3 Analog-to-Digital Conversion

In order for the FPGA to process analog signals, analog-to-digital conversion must take place. The signals that need to be converted from analog-to-digital are the control knob voltages on the T_x and the amplified output voltage of the colour detector on the R_x .

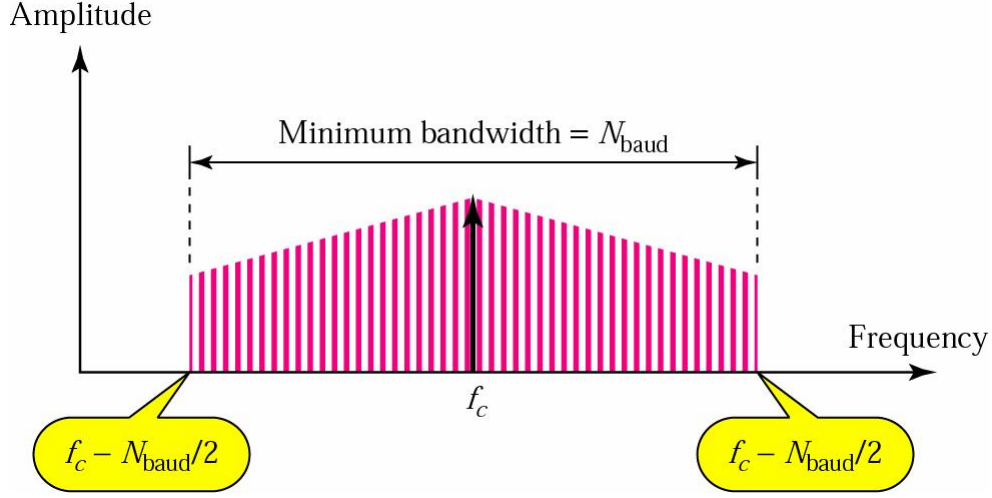


Figure 11: Determining MPSK/QAM Bandwidth: Requires a center frequency and the system baud rate.

4.3.1 Transmitter

As the voltage change of the control knobs will be relatively slow (based on how quickly a user can rotate the knobs), using a serial ADC was sufficient to capture the output voltages from the rotation of the linear potentiometers. The selected ADC was the four channel TLV0834 [24]. It was suitable due to its 3V operating voltage, 8-bit resolution, low supply current and compatibility with TTL logic. Three of the four channels of the TLV0834 were used for the three control knobs, with the fourth channel tied to GND. The required control signals ($\overline{\text{CS}}$, CLK and DI) and output signals (SARS and DO) were connected to respective output and input lines to the FPGA [21].

4.3.2 Receiver

The three input signals from the colour detectors required to be processed simultaneously and in parallel, such that the delay between them would be kept to a minimum. The input signals would be changing rapidly, therefore a high speed ADC was required. To be able to receive data simultaneously from all three ADCs, it required that they all share the same clock (CLK) and output enable ($\overline{\text{OE}}$) signals. The selected ADC was the TLC5540 [25],

a high speed 8-bit resolution ADC which allowed sample conversions to be read on every falling edge of the supplied CLK. The TLC5540 has a scalable reference voltage range, suitable for this project as it must be adjusted to suit the DC offset of the colour detector variable gain stage.

The reference voltage on the ADC was designed such that a 2V full scale voltage range was achieved between +1.5V and +3.5V. The internal resistors provided by the TLC5540 were not sufficient to achieve this range, thus two external 200Ω resistors were added to bias the ADC correctly (see Figure 12).

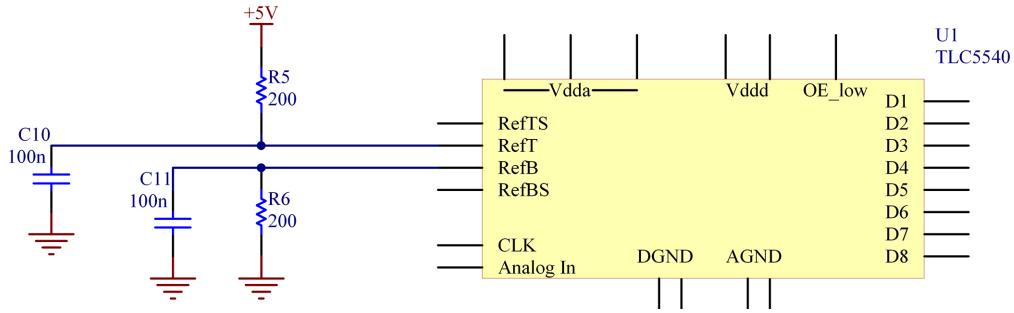


Figure 12: TLC5540 Reference Voltage Biasing

To determine the value of the resistors, the datasheet supplied a typical value of 7.5mA of current passing through the 270Ω reference resistor inside the device [25]. With a +5V supply, REFT and REFB were calculated as:

$$\begin{aligned}
 I_{ref} &= 7.5\text{mA} \\
 R_{ref} &= 270\Omega \\
 V_{ref} &= 2.0\text{V} \\
 R_{refT} &= \frac{5.0 - 3.5}{7.5\text{mA}} \\
 &= \frac{1.5}{7.5\text{mA}} \\
 &= 200\Omega
 \end{aligned}$$

$$\begin{aligned}
R_{refB} &= \frac{5.0 - 1.5 - V_{ref}}{7.5\text{mA}} \\
&= \frac{1.5}{7.5\text{mA}} \\
&= 200\Omega
\end{aligned}$$

The TLC5540's digital logic levels were different to the maximum supported by the S3EDK, therefore logic translation was required for both the input and output digital signals sent to the device [26, 27, 28]. Logic translation devices are used to allow devices with different voltage level inputs and outputs to communicate. For this project, the TXB0104 [29] bi-directional logic translator was chosen for its simple connection and ease of use. The device did not require additional directional flags to be sent to the device (thus conserving valuable S3EDK IO lines) and could cater for up to 100MSPS.

4.4 Digital-to-Analog Conversion

To be able to decode the binary output data produced by the FPGA into an analog format suitable for the colour driver and audio tone output, digital-to-analog conversion must take place. The T_x and R_x use different format DACs, with each DAC having a separate architecture better suited for its specific application.

4.4.1 Transmitter

In this project, the simultaneous transmission of different coloured LEDs to produce different colours required that a fast, parallel DAC be used to drive the colour circuitry. For this task, the AD7801 was chosen [30]. To be able to transmit data simultaneously, it required that all three DACs share the same chip select ($\overline{CS}$) and write select ($\overline{WR}$) signals. The LDAC pin is tied to GND, allowing continuous conversions to take place based on the rising edge of $\overline{WR}$ [31]. The digital timing for each bit word to begin conversion is 80ns, or 12.5MHz.

4.4.2 Receiver

Generating audible tones from digitally synthesised bistreams was achieved using a low cost stereo audio DAC. The selected DAC was a $\Delta\Sigma$ modulator with an $8\times$ oversampling rate, the PCM1744 [32, 33]. The audio data was to be serially clocked with the FPGA using the Phillips I²S format [34] (binary 2's complement), and with a maximum of 24 bits per channel. The sampling frequency range of the DAC ranges from 16kHz to 96kHz, with the master clock operating at $256\times$ the sampling frequency. The supply voltage V_{cc} for the DAC is +5V, with the analog center voltage at $V_{cc}/2 \Rightarrow 2.5V$, and the full scale peak-to-peak voltage, $0.62 \times V_{cc} \Rightarrow 3.1V$.

For this project, the selected sampling frequency, f_s , was 19.531kHz (LRCIN), resulting in a system clock (SCKI) of 5MHz. The I²S data input timing diagram for the device shows that the bit clock (BCKIN) for placing the audio data into the PCM1744 is $64\times f_s \Rightarrow 1.25MHz$.

4.5 Colour Drivers

The design for the colour drivers uses LEDs as discussed in Chapter 3. Based on the feasibility report in Chapter 2, the required number of red LEDs was 40, green LEDs was 20 and blue LEDs was 6. In this design, current feedback operational amplifiers (opamps) are used to regulate the current through the LEDs [35, 36]. By varying the voltage at the positive input of the opamp, the current regulated through the feedback resistor will change, thus causing the intensity of the LEDs to change (see Figure 13).

To determine how many LEDs were placed on the output of the opamps, the datasheet [37] for the LEDs were used as well as some empirical tests using a CRO. The results of the tests and the comparable datasheet specifications are presented in Table 13.

By using the +12V supply rail and a maximum of 1V for V_p of the current feedback opamp, a maximum of 11V was available for the opamp to drive its output in order to maintain 1V across the feedback path. This design decision

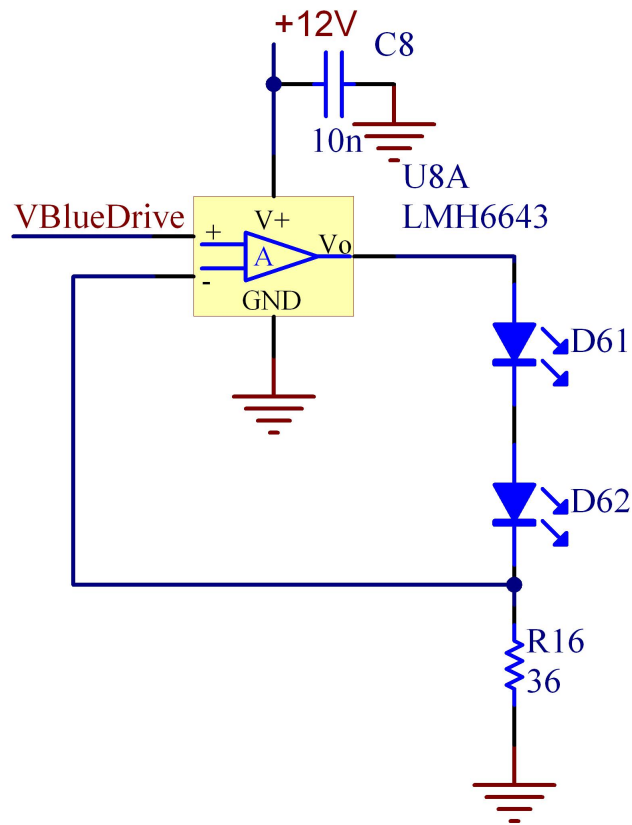


Figure 13: Current Feedback Op Amp for LED Circuitry

LED	Experiment Result	Datasheet Specification
Red	2.0V	2.3V
Green	3.2V	3.5V
Blue	4.0V	3.5V

Table 13: Foward Voltage Drop of 10000mcd LEDs

demands that the current feedback opamp be rail-to-rail. As a result of this condition, the LMH6643 low power rail-to-rail current feedback operational amplifier was chosen [38].

The LMH6643 has a typical output swing to within 25mV of the rail and a maximum of 75mV, as well as supply a drive current of 75mA. The device is also able to operate on a single supply of +12V and typically requires 2.7mA of supply current. Using Table 13, the quantity of LEDs to be placed on each output (to ensure safe operation) is presented in Table 14.

LED	Number of LEDS	Number of Opamps Required
Red	5	8
Green	3	7
Blue	2	3

Table 14: Number of RGB LEDs in Opamp Path

The transmitter DAC has a full scale output voltage equivalent to V_{cc} , thus the output of the DAC required a voltage divider from 5V to 1V. The resistor values for the DAC output voltage divider was calculated as:

$$V_o = \frac{R_2}{R_1 + R_2} \cdot V_{in}$$

$$R_2 = 0.2(R_1 + R_2)$$

$$0.8R_2 = 0.2R_1$$

$$\therefore R_1 = \frac{0.8}{0.2}R_2 = 4R_2$$

$$\therefore R_1 = 4k \Rightarrow 3.9k\Omega \text{ using E24 values}$$

$$R_2 = 1k \Rightarrow 1.0k\Omega \text{ using E24 values}$$

Checking...

$$\begin{aligned} V_o &= \frac{1k}{3.9k + 1k} \cdot 5.0 \\ &= 1V \end{aligned}$$

As a result of the voltage divider, when the T_x DAC is loaded with 0xFF, the effective input voltage to the colour driver opamps will be 1V. When the DAC is loaded with 0xC0, the input voltage to the opamps will be 750mV. The feedback resistor in Figure 13 is 36Ω . This resistor value will ensure that 27.7mA will be passing through the LEDs when the T_x DAC is loaded with 0xFF. The maximum output current is based on Chapter 2 experiments.

4.6 Colour Detection

The foundation for the colour detection circuitry was that it must decouple ambient light. The project defined ambient light as slow changing light, effectively being a DC component. Using the EPIGAP photodiodes discussed in Chapter 2, an AC coupled colour filter was designed such that ambient light from sunlight and fluorescent tubes would not impact on the ability for the circuit to discriminate between colours. Taking into account the projected $1\mu A$ response of the photodiodes, the circuit would also require amplification to enable the receiver ADC to convert the detected signal in the range of 1.5V and 3.5V. Conversion of the signal using the TLC5540 provides the necessary DC biasing condition of the last stage in the filter design and the effective peak-to-peak amplitude of the final voltage.

To design the filter, a central frequency of 50kHz was selected with the lower bound of the filter one decade lower at 5kHz, and the upper bound one octave higher at 100kHz. The wide passband in this filter criteria provides a large bandwidth for the system to use a modulation technique to embed data in the colour transmission using MPSK or QAM. In considering filter topologies, a Sallen-Key active filter configuration was chosen as simultane-

ous amplification of the filtered signal is possible. To design the filters, it was required to design the photodiode biasing such that an input voltage to the first filter stage was known.

As the photodiodes needed to be DC biased, the maximum DC saturation current of the photodiodes needed to be determined. The maximum DC saturation current produced by these photodiodes would be when they were placed in direct sunlight. The Sun's radiant energy is approximately 1000Wm^{-2} on the earth's surface [39], thus approximately 0.001Wmm^{-2} . Using the active area and responsivity specifications of the EPIGAP photodiodes from their respective datasheets [40, 41, 42], the maximum saturation current was calculated (see Table 15) so that an appropriate DC bias level could be found.

Photodiode	Active Area	Responsivity	Energy from Sun	DC $I_{\text{SAT}_{\text{max}}}$
Red	0.13mm^2	0.42A/W	$130\mu\text{W}$	$54.6\mu\text{A}$
Green	1.2mm^2	0.25A/W	1.2mW	$300\mu\text{A}$
Blue	1.2mm^2	0.30A/W	1.2mW	$360\mu\text{A}$

Table 15: Photodiode Maximum DC Saturation Current

With the combined results of Table 15 and the results of finding an appropriate DC biasing resistor (see Table 16), the photodiodes were designed such that they would conduct even in a saturated state, and the input voltage for the filter circuit for a $1\mu\text{A}$ photodiode current would be 10mV .

Photodiode	R_L 50Ω	R_L $1\text{k}\Omega$	R_L $10\text{k}\Omega$
Red	2.73mV	54.6mV	546mV
Green	15mV	300mV	3.0V
Blue	15mV	360mV	3.6V

Table 16: Photodiode DC Biasing Resistor Choices

Having determined the minimum input voltage for the filter circuits, the Sallen-Key active filters could be designed. A 3rd order Butterworth design was implemented with the aid of the Filter Pro software package [43] for both the high pass and low pass components of the wideband filter. The software

package did not account for DC biasing of the opamps, thus appropriate resistor values replaced those specified by the software package. The resultant filter design for the red and green colour detectors is shown in Figure 14, while the blue detector filter design is shown in Figure 15.

The Sallen-Key filter design provided only a fixed amount of gain for each colour detector, thus making it difficult to detect changes in amplitude if QAM was used to modulate the embedded data. A solution to this was to design a variable gain amplifier (VGA) stage before the detected signal was converted by the R_x 's ADC. The VGA output could then be monitored by the FPGA and the gain modified in a linear manner if not suitable.

In this design, a digital potentiometer was used as the variable gain component in the ADC pre-amplifier (see Figure 16). The transfer function for this VGA is governed by:

$$A_g = \frac{V_{out}}{V_{in}} = 1 + \frac{R_F}{R_L} \quad (5)$$

Equation 5 is dependant on the resistor in the feedback path, R_F , and the parallel combination of the load resistance that biases the negative terminal of the opamp, R_L . R_F in this design is a 256 step, $10k\Omega$ digital potentiometer, the AD8400 [44]. The transfer function to calculate the resistance per AD8400 step for the terminal and wiper configuration shown Figure 16 is:

$$R_{WB}(\Delta s) = \left(\frac{\Delta s}{256} \cdot 10k\Omega \right) + 50\Omega \quad (6)$$

The combination of Equation 5 and Equation 6 was used in a C++ program [45] to list the achievable gain for differing combinations of R_L . The output of this program was analysed to determine that an R_L of 500Ω would provide sufficient gain for each colour detector circuit, as $1.1 \leq A_g \leq 21.0219$ [46]. To provide DC opamp biasing on the negative feedback path and fulfil the criteria of R_L , two $1k\Omega$ resistors were used in parallel. For completely gain independant DC opamp biasing, the positive input to the opamp used two

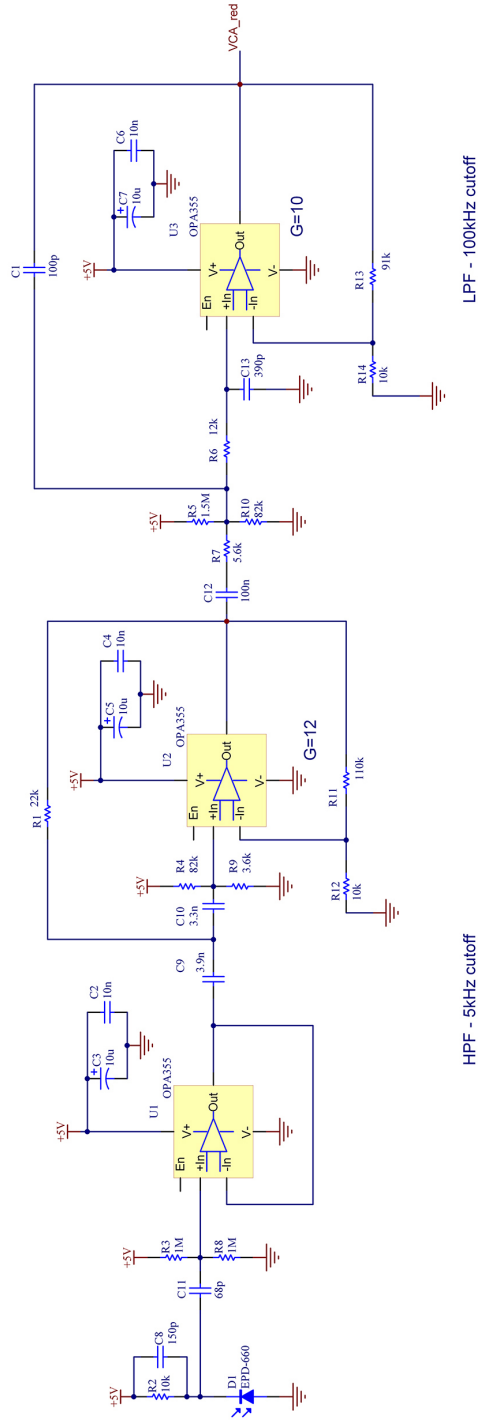


Figure 14: 3rd Order Sallen-Key Active Filter for Red and Green Colour Detection. The first stage is a HPF with $f_c = 5\text{kHz}$, the second stage is a LPF with $f_c = 100\text{kHz}$.

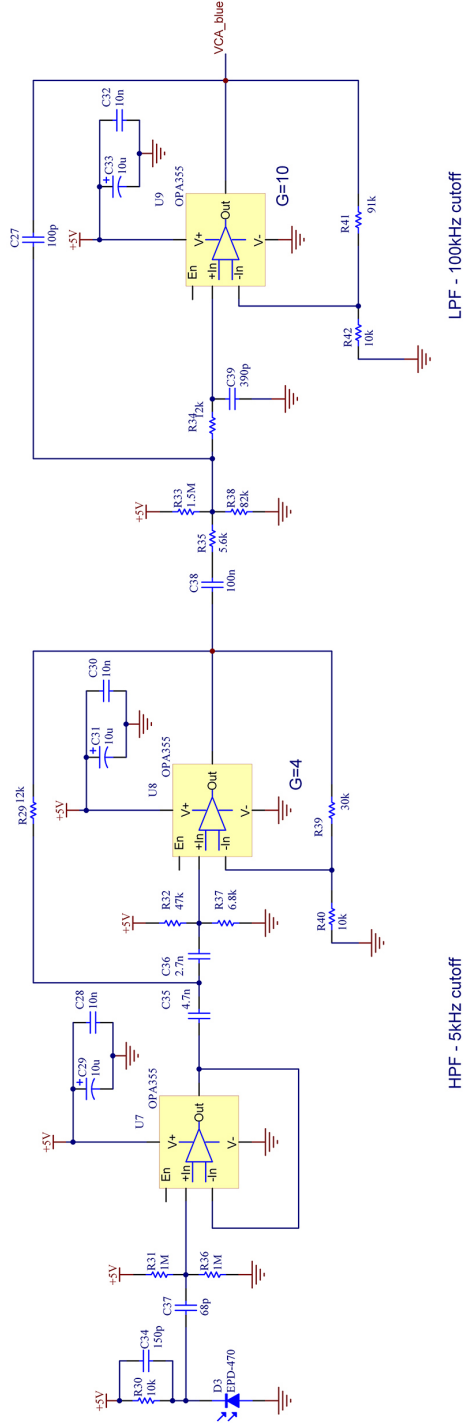


Figure 15: 3rd Order Sallen-Key Active Filter for Blue Colour Detection. The first stage is a HPF with $f_c = 5\text{kHz}$, the second stage is a LPF with $f_c = 100\text{kHz}$.

input bias current, low noise, rail to rail output and preferably a high slew rate. The OPA355 was the chosen opamp for this design [47, 48, 49, 50, 51].

4.7 Audio Output

The R_x module's audio output stage was required to have audible output via powered speakers or a mixing desk. To determine if a pre-amplifier was required for the output stage, an empirical approach was taken to determine if the output voltage levels of the audio DAC would be sufficient to drive the inputs to standard mixing consoles available in many auditoriums.

This empirical approach used a Roland DJ1000 professional DJ mixer [52] to ascertain the minimum input voltage required for the R_x module's output stage. The input signal to the mixer (via a line-in channel) was a 1kHz sine wave, and its peak-to-peak voltage was varied based on the DJ1000's input gain level. The mixer's input gain level was adjusted from minimum to maximum, and the input signal's amplitude was varied such that the signal reached the 0dB mark on the mixer's post fader indicator. The results are presented in Table 18.

Gain Level	Gain Description	Voltage Required
0	No gain control	$4.0V_{pp}$
5	Standard gain control	$2.0V_{pp}$
10	Full gain control	$240mV_{pp}$

Table 18: R_x Audio Output Voltage for Mixer Input

The PCM1744 specification stated that the full scale output voltage swing was $0.62 \times V_{cc}$, thus the output voltage swing with V_{cc} at 5V was $0.62 \times 5.0V = 3.1V_{pp}$. Based on the empirical results from Table 18 and comparisons with other popular mixing console datasheets [53, 54, 55], it was determined that the output of the PCM1744 would be sufficient to supply mixing desks.

To offer protection to the audio DAC circuitry and to isolate the output signal, a buffer is placed between the audio DAC's left and right channel outputs and the physical RCA connectors [33]. Each of the voltage follower

op-amps is DC biased at the central frequency of the PCM1744, specified at $V_{cc}/2 \Rightarrow 2.5V$. This will ensure that whatever connects to the output of the circuit will have no effect on the circuit itself. Each buffer has a 51Ω bleed resistor in series with the $10nF$ output capacitor to reduce turn on “pop” when connecting external devices to the R_x ’s audio output.

4.8 Power

An initial design constraint for both the transmitter and receiver was that they were to be accessible from any mains power supply. To reduce the overall board space of constructing an AC/DC power supply for both the transmitter and receiver, two 12V 4A DC regulated switchmode power supplies (PSU) were used as the top voltage supply rail for both circuits. This decision put a constraint on the system wide design, that the highest voltage rail was at 12V DC, and able to supply a maximum of 48W. Using a switchmode power supply would add an amount of high frequency switching noise to the system, however, this solution reduced overall complexity and cost of the system design and switching noise is compensated for by using decoupling capacitors on devices.

In order to facilitate the protection of the devices on each of the two boards in case of applying a reverse voltage by the end user, the +12V DC rail required a schottky diode to provide protection. The choice of the diode required to a minimum 4A diode with a low forward voltage drop, as a high forward voltage drop would impact on the available voltage that could be used as a top rail. Although not a concern for the receiver, the transmitter was heavily reliant on the +12V rail due to the colour driving circuit. The 50WQ03FN 5.5A Schottky Barrier diode was chosen for it’s low forward voltage drop of 0.35V at 5A, as well as its small, surface mountable package [56, 57].

A +5V supply was required for a number of components on the T_x and R_x modules. Requirements for the +5V regulator were steady supply current, low noise and in input voltage maximum at least equal to the +12V rail. The L7805 +5V linear regulator was chosen for its low cost, high input voltage,

steady output current and high current supply [58]. Low thermal resistance heatsinks [59] with silicon heatsink compound were used to dissipate the heat generated by the regulator [56, 57].

As with the +5V supply, the specification for the +3.3V supply for the T_x and R_x modules was the same. The LM117DT-3.3 regulator was chosen [60] for these modules. In a small, surface mountable package that did not require a heatsink; the device's temperature stability, low drop-out voltage and similarity to the LM317 made it a suitable choice [56, 57].

Power budgets for the T_x and R_x modules were calculated using the selected components for the design. For the power budgets, only IC devices are considered, as the power required for pull up/down resistors, biasing resistors is negligible. The power budget for the T_x module is presented in Table 19, while Table 20 presents the power budget for R_x module.

Device	+3.3V	+5.0V	+12.0V	Comment
L7805	0.75mA	10mA 2.5mA	6mA	I_d max
LM1117DT-3.3				I_d max
AD7801 ($\times 3$)				I_{cc} max
TLV0834				I_{cc} max
LMH6643 ($\times 18$)			5.5mA	I_s
LEDs ($\times 18$)			27.7mA	I_{drive}
Totals	0.75mA	17.5mA	605mA	
Power per rail	2.475mW	87.5mW	7.26W	

Table 19: Power Budget for T_x

From Table 19, the total power required from the PSU was 7.35W assuming 100% efficiency of the unit. Using a conservative estimate of 80% efficiency for the PSU, the Σ Power required was 9.19W. For the T_x , this is well within the 48W that the PSU is able to supply.

From Table 20, the total power required from the PSU was 1.67W assuming 100% efficiency of the unit. Using a conservative estimate of 80% efficiency for the PSU, the Σ Power required was 2.09W. For the R_x , this is well within the 48W that the PSU is able to supply.

Device	+3.3V	+5.0V	+12.0V	Comment
L7805			6mA	I_d max
LM1117DT-3.3		10mA		I_d max
OPA355 ($\times 14$)		14mA		I_{cc} max
PCM1744		18mA		I_{cc} max
TLC5540 ($\times 3$)		27mA		I_s
AD7801 ($\times 3$)		4mA		I_{out}
TXB0104 ($\times 7$)	5 μ A	5 μ A		I_{out}
Totals	35 μ A	317mA	6mA	
Power per rail	115.5 μ W	1.6W	72mW	

Table 20: Power Budget for R_x

4.9 Firmware

The system level firmware design for the T_x and R_x modules was required to provide the communication between devices and generate the driving logic for fulfilling the functional description of the modules.

The firmware for the T_x is primarily responsible for handling the user input and generating an appropriate output transmission bit stream to be sent to the colour driver circuit. A top level description of these components is presented in Figure 17.

The firmware for the R_x is responsible for performing colour discrimination on the incoming coloured transmission signal, as well as use DSP techniques to create an audible tone based on the discriminated colour. Using a numerically controlled oscillator or direct digital synthesiser, the R_x module must produce frequency selectable output tones to be sent to the audio DAC. A top level description of these components is presented in Figure 18.

4.10 Summary

In this chapter, a thorough documentation of the design procedure for this project was presented. This design used the results from the feasibility study in Chapter 2 combined with the project analysis of Chapter 3, to construct a physically realisable implementation of the project objectives detailed in

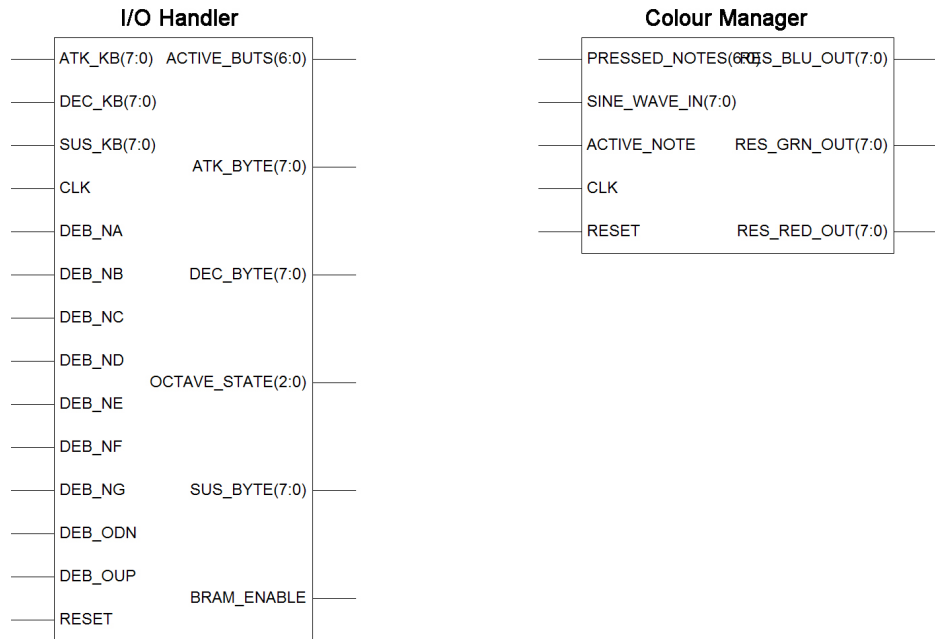


Figure 17: Top Level Description of T_x Firmware Components

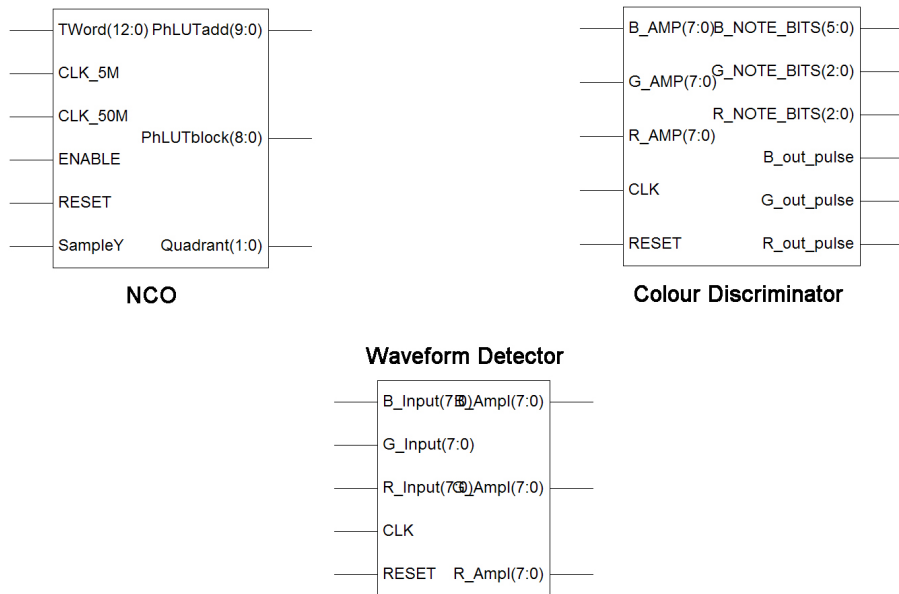


Figure 18: Top Level Description of R_x Firmware Components

Chapter 1. In addition to presenting the design methodology in terms of critical project objectives, this chapter also described the addition of components and design strategies to allow the project to be able to fulfill its desirable objectives.

This chapter used mathematical modelling, computer software and values supplied by component vendors to approximate a functional and component based system design. In the next chapter, we present simulation procedures that are designed to assist in validating these design choices and serve to provide a reference when testing the system implementation.

5 Simulation

In the previous chapter, the component based design for implementing a physical realisation of the project objectives was outlined. The chapter described the electronic considerations for producing and detecting colour information that could be converted to an audible tone using DSP techniques in an FPGA.

In this chapter, we present the simulation procedure that were designed to assist in validating the design choices and to serve as a reference when testing the system implementation. The chapter describes the simulation of the analog filters used for colour discrimination and the firmware required to communicate with digital devices and provide digital functionality for implementing the project.

5.1 Analog Filters

From Chapter 4, the colour detection filter circuits for the red and green photodiodes were the same, while the blue filter design had a lesser overall achievable gain. Both circuits were simulated using the freely available TINA PSpice simulation software. A TINA simulation macro model for the OPA355 was available from the vendor, and was in the simulation design. By using the vendor supplied simulation model for the device, a more accurate prediction of the physical response of the filter circuit with respect to voltage outputs and amplitude vs frequency responses was expected. Figure 19 depicts the TINA simulation circuit for the red and green filters, while Figure 20 depicts the TINA simulation circuit for the blue filter.

AC nodal voltage analysis was performed on each simulation circuit to determine the expected DC and peak-to-peak output voltage levels from both minimum and maximum photodiode input currents. The nodal points are marked N1, N2, N3, N4 and N5 in both Figure 19 and Figure 20. The input signal to each simulation was a 50kHz sinusoidal wave with a varied amplitude dependant on the simulation being performed. The value for R_F in the

VGA stage of the filter circuits was varied dependant on the simulation being performed, however, the value used was derived from Equation 6, in order to satisfy a 2V amplitude on N5 [46].

Table 21 and Table 22 present the red filter simulation results for 250nA (minimum) and $1.1\mu\text{A}$ (maximum) input signals respectively. Table 23 presents the green filter simulation result for a $1.2\mu\text{A}$ (maximum) input signal, as the minimum 250nA input signal is presented in Table 21. Table 24 and Table 25 present the red filter simulation results for $1\mu\text{A}$ (minimum) and $4.5\mu\text{A}$ (maximum) input signals respectively. The simulation results provided a higher level of confidence that the design would perform as expected, with physical testing used to verify these results.

Node	DC Level	Amplitude
N1	2.50V	2.16mV
N2	2.50V	2.16mV
N3	2.53V	26.1mV
N4	2.62V	250.31mV
N5	2.51V	2.0V

Table 21: TINA AC Nodal Analysis – Red/Green Filter: 250nA input current, $R_F = 3487.50\Omega$ (R19)

Node	DC Level	Amplitude
N1	2.50V	9.52mV
N2	2.50V	9.52mV
N3	2.53V	114.83mV
N4	2.62V	1.10V
N5	2.50V	1.99V

Table 22: TINA AC Nodal Analysis – Red Filter: $1.1\mu\text{A}$ input current, $R_F = 401.5625\Omega$ (R19)

The TINA PSpice simulation package was also used to characterise the AC amplitude response of the filter circuits over the given pass band frequencies that they were designed for. The results of the simulation are presented in Figures 21 – 28 for both the red/green and blue filter circuits. The resultant graphs are an important simulation step as they show the frequencies outside

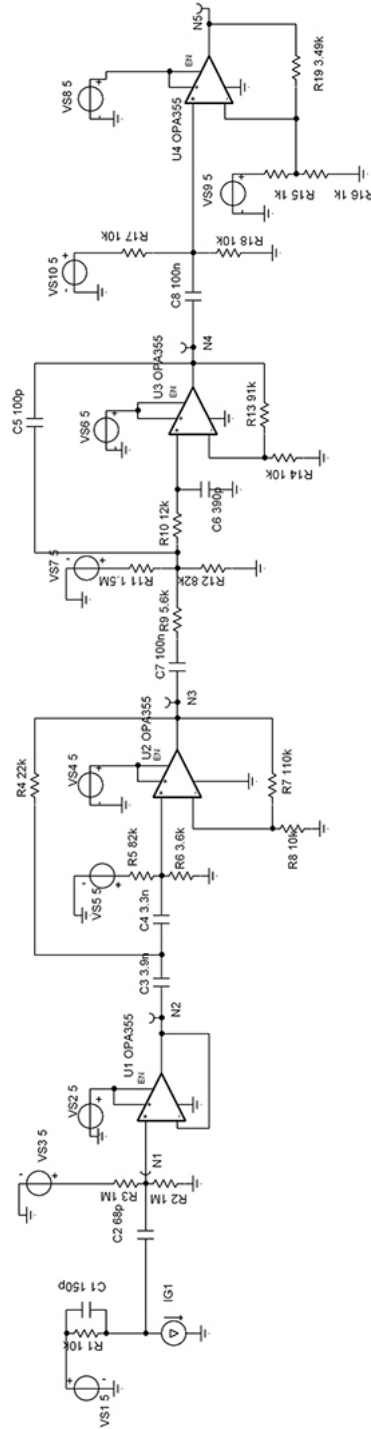


Figure 19: TINA PSpice Simulation Circuit for Red and Green Filters

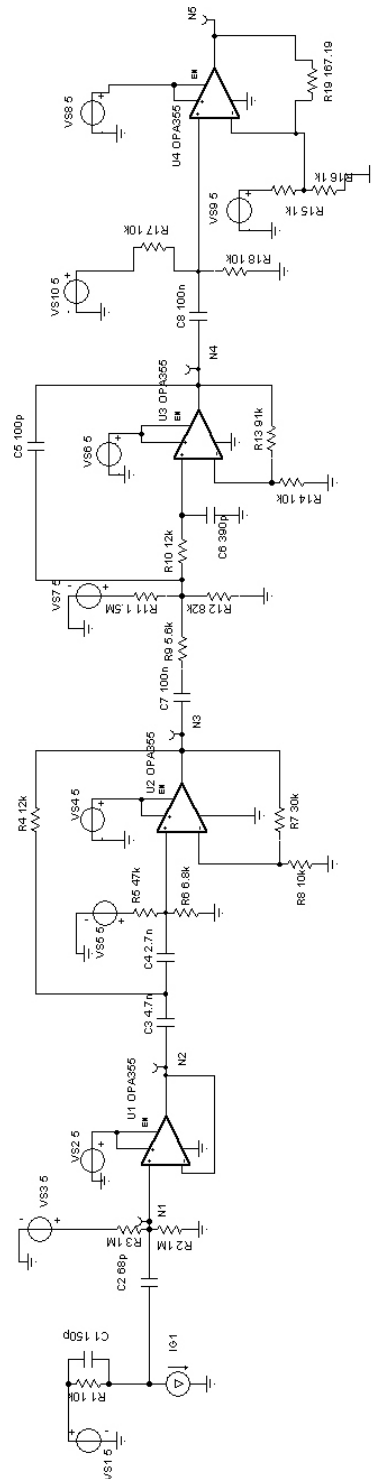


Figure 20: TINA PSpice Simulation Circuit for Blue Filter

Node	DC Level	Amplitude
N1	2.50V	10.39mV
N2	2.50V	10.39mV
N3	2.53V	125.27mV
N4	2.62V	1.20V
N5	2.50V	1.98V

Table 23: TINA AC Nodal Analysis – Green Filter: $1.2\mu\text{A}$ input current, $R_F = 323.4375\Omega$ (R19)

Node	DC Level	Amplitude
N1	2.50V	8.66mV
N2	2.50V	8.66mV
N3	2.53V	34.66mV
N4	2.62V	332.46mV
N5	2.51V	2.00V

Table 24: TINA AC Nodal Analysis – Blue Filter: $1.0\mu\text{A}$ input current, $R_F = 2510.9375\Omega$ (R19)

Node	DC Level	Amplitude
N1	2.50V	38.96mV
N2	2.50V	38.97mV
N3	2.53V	155.98mV
N4	2.62V	1.50V
N5	2.50V	2.00V

Table 25: TINA AC Nodal Analysis – Blue Filter: $4.5\mu\text{A}$ input current, $R_F = 167.1875\Omega$ (R19)

the designed 5kHz–100kHz range that could be used for AC modulation, and characterise the amount of attenuation for the DC frequencies.

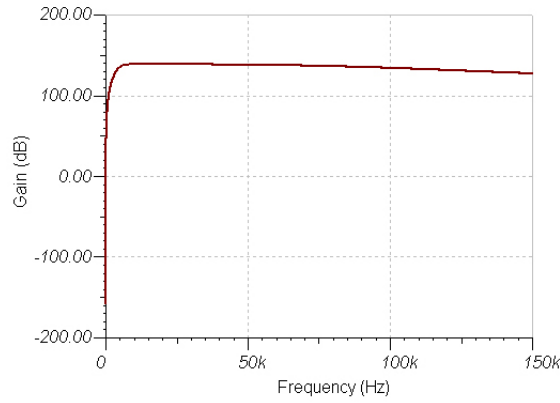


Figure 21: TINA PSpice Bode Plot Red/Green Filter for 1Hz - 150kHz range

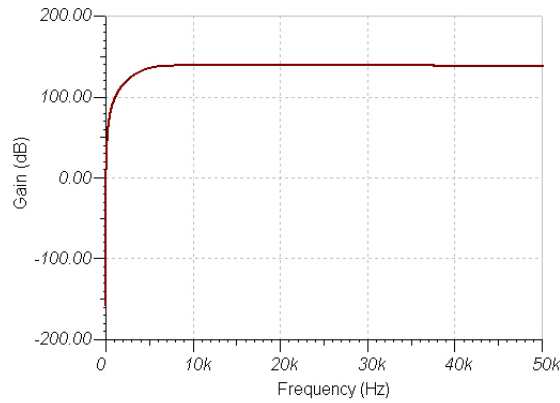


Figure 22: TINA PSpice AC Amplitude Response Red/Green Filter for 1Hz - 50kHz range

The results of the TINA PSpice AC amplitude transfer characteristics for all three colour detector circuits provided a higher level of confidence that once constructed, the filters would be sufficiently AC coupled, with ambient light not impacting on colour detection. The plot of Figures 21 – 28 will be verified with testing once the circuit is constructed.

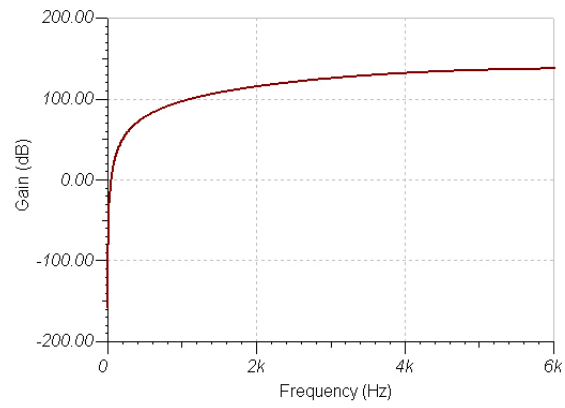


Figure 23: TINA PSpice AC Amplitude Response Red/Green Filter for 1Hz - 6kHz range

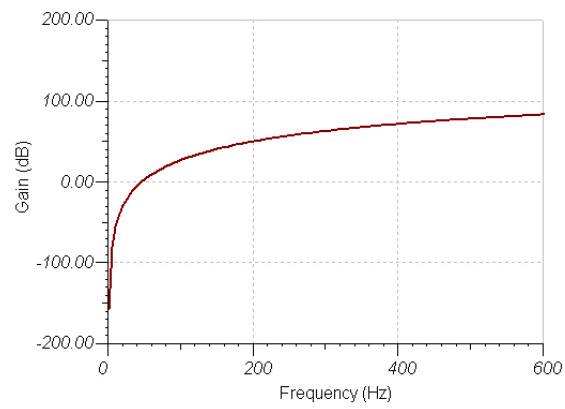


Figure 24: TINA PSpice AC Amplitude Response Red/Green Filter for 1Hz - 600Hz range

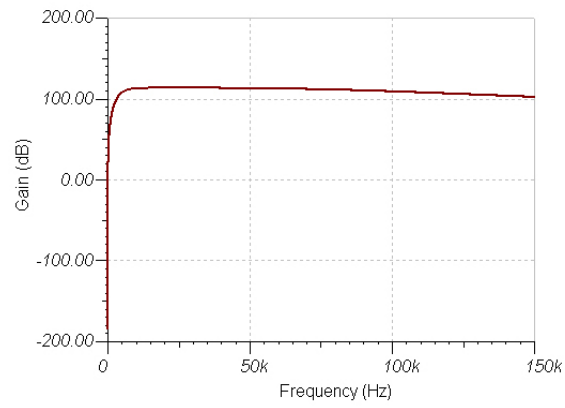


Figure 25: TINA PSpice AC Amplitude Response Blue Filter for 1Hz - 150kHz range

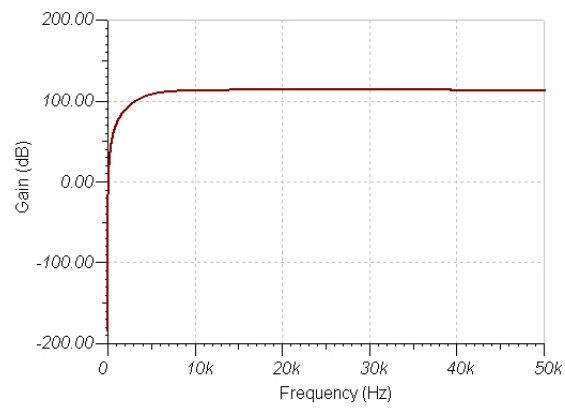


Figure 26: TINA PSpice AC Amplitude Response Blue Filter for 1Hz - 50kHz range

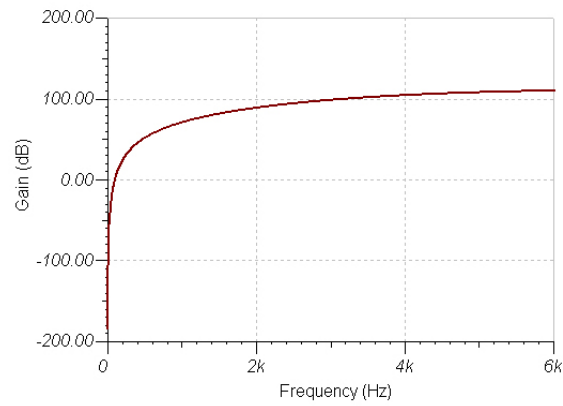


Figure 27: TINA PSpice AC Amplitude Response Blue Filter for 1Hz - 6kHz range

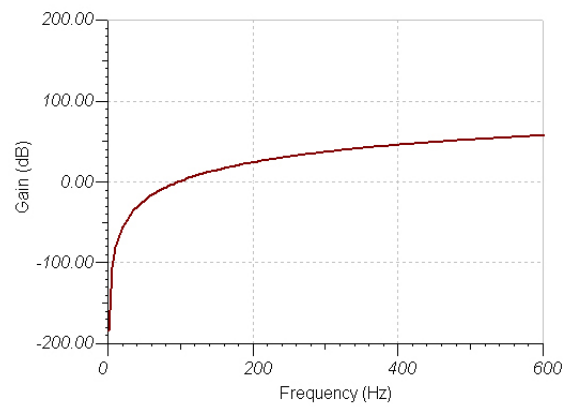


Figure 28: TINA PSpice AC Amplitude Response Blue Filter for 1Hz - 600Hz range

5.2 Firmware

Firmware simulation utilised the ModelSim software package, enabling the visualisation of VHDL implementations of device specific timing requirements. The firmware implementations for all devices were simulated based on timing diagrams within their respective datasheets. ModelSim was also used to simulate the logical constructs that implemented the functionality of the project's two modules.

5.2.1 Device Timings

Simulation of the digital device timings was an imperative step to meeting the critical project objectives. Simulation results of the individual devices could be confirmed once the project modules were constructed then tested. The device timing simulations in Figures 29 – 34, were successful in achieving the minimum criteria for digital timings, and a comparison to individual datasheets will confirm the simulation success.

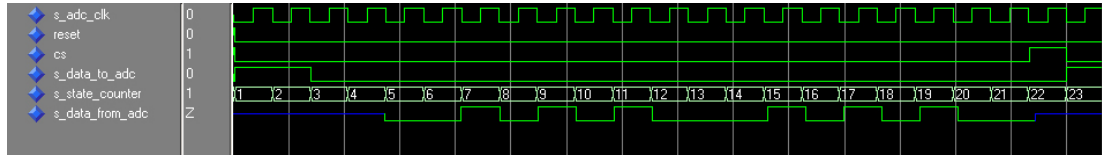


Figure 29: ModelSim T_x ADC Simulation [24]

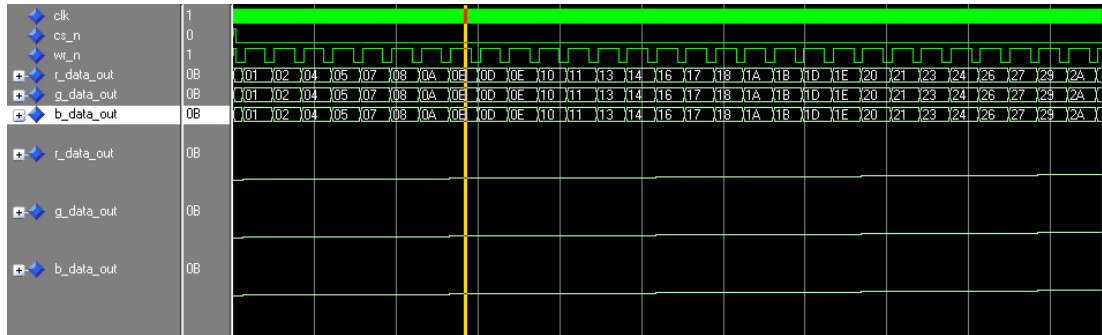


Figure 30: ModelSim T_x DAC Simulation – Bit View [30]

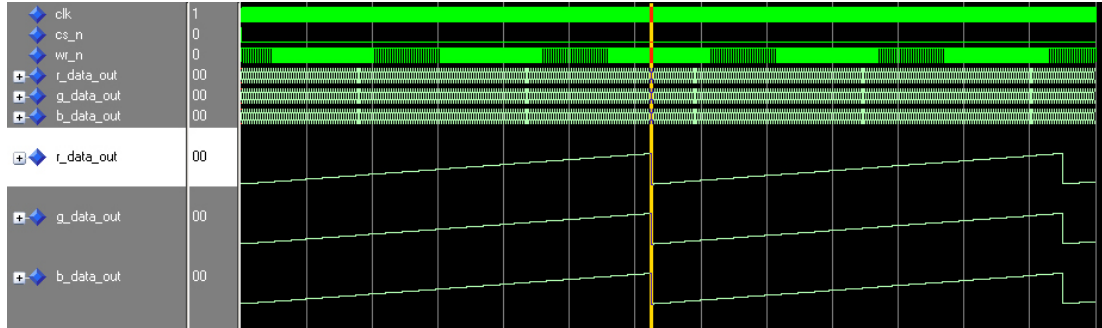


Figure 31: ModelSim T_x DAC Simulation [30]

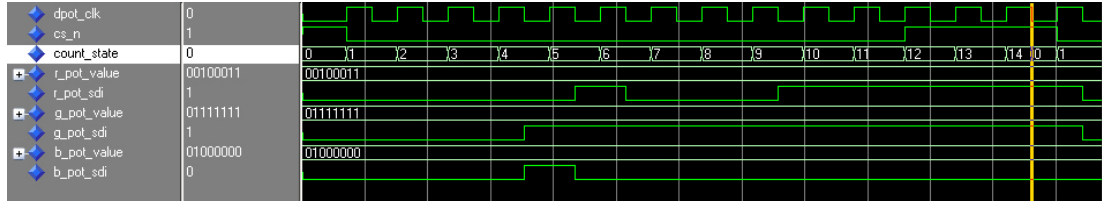


Figure 32: ModelSim R_x Digital Potentiometer Simulation [44]

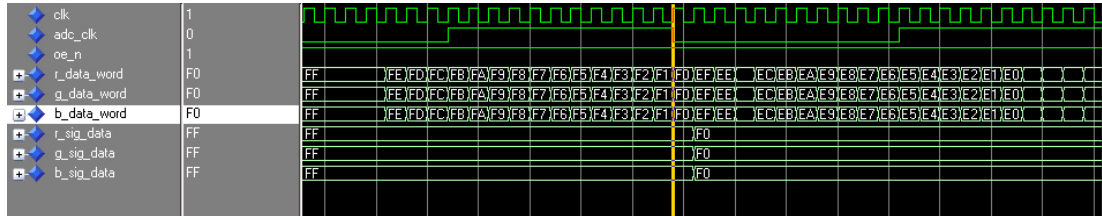


Figure 33: ModelSim R_x ADC Simulation [25]



Figure 34: ModelSim R_x DAC Simulation [32]

5.2.2 Logic Flow

The logical constructs that brought together the functionality of the individual components and fulfilled the functionality of the project design were also simulated. Simulating the logical constructs individually would assist in the methodical implementation of the resultant firmware, provide a better approximation to expected result, and would be invaluable if debugging was required.

Firmware based debouncing was simulated to confirm proper operation. As the main interface for user interaction, this component required to be fully functional (see Figure 35). The T_x transmission control logic was also simulated to confirm that access to the FPGA's block RAM when used as a sine look up table was successful. The values inserted into the block RAM were created using a C++ program to increase productivity [61]. Figures 36 and 37 confirm that the access to the block RAM was successful, resulting in a sinusoidal output bit stream.

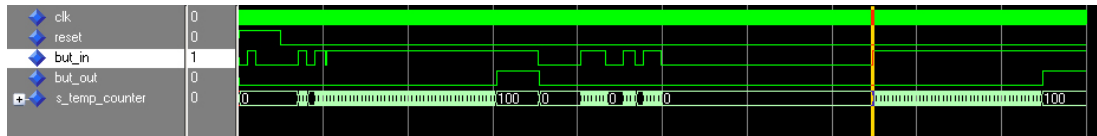


Figure 35: ModelSim T_x Debounce Simulation

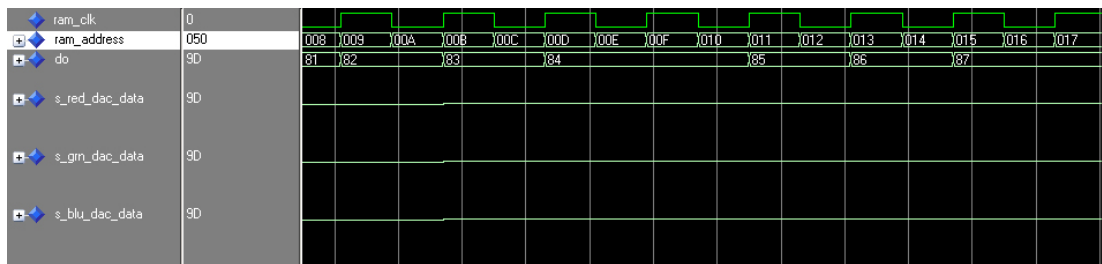


Figure 36: ModelSim T_x Sine Wave Simulation – Bit View

Simulation of the numerically controlled oscillator (NCO) for tone generation on the R_x module encapsulated many components (see Figure 38). The resultant output signal from the NCO module was used to provide the input

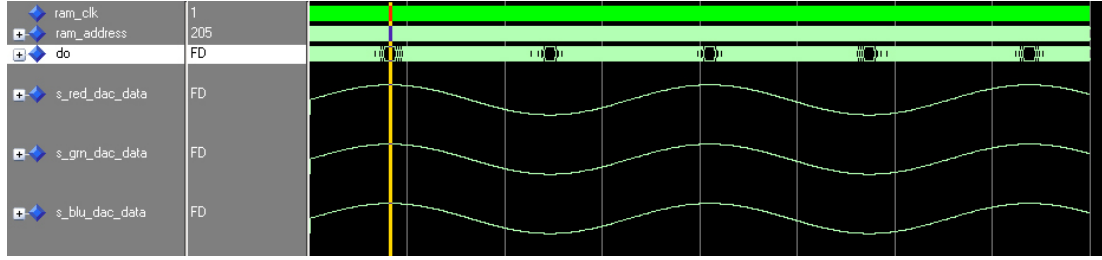


Figure 37: ModelSim T_x Sine Wave Simulation

stimulus for the audio DAC bitstream in Figure 34. The NCO used block RAM to access a large look up table based on phase increments rather than frequency steps. The values for the phase increments were generated using a C++ program to efficiently initialise the FPGA block RAM [62].

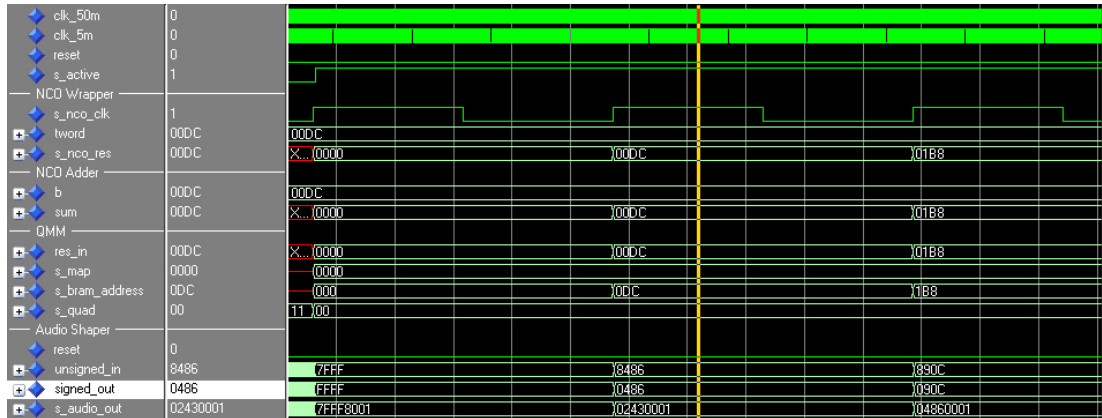


Figure 38: ModelSim R_x NCO Simulation

5.3 Summary

In this chapter, we presented the simulation procedures used to verify and corroborate the project design from Chapter 4. The simulation procedures used software to more accurately predict the resultant output of the finally constructed circuit and firmware. The analog filters were simulated with minimum and maximum expected photodiode input currents and resultant output voltages for output stages were presented. The amplitude frequency

response of the filter circuits was also simulated outside the designed frequency range, thus demonstrating the possible application of the filter circuit to QAM modulation. FPGA firmware was also simulated, with digital device timings meeting vendor specifications and logical constructs developed to alleviate integration problems and issues with block RAM access.

For simulation and design to be tested, the project must be physically realised through construction. In the next chapter, the construction of the design detailed in Chapter 4 is presented.

6 Construction

In this previous chapter, we presented simulation procedures used to verify and corroborate the project design. The simulations would be used as a reference during testing of the physical implementation of the design. In this chapter, the construction of the design detailed in Chapter 4 is presented. The physical layout of the components and physical design considerations are discussed and detailed with respect to the T_x and R_x modules.

The T_x and R_x module consist of four printed circuit boards (PCBs) in total; two for the T_x and two for the R_x . Each module can be classified as consisting of a motherboard and daughterboard. The physical design of the modules used the motherboard and daughter board classification to separate the main functionality into two sections.

For the T_x , the motherboard consisted of [63]:

- The user interface: the user keys, octave shifter and control knobs; and
- The digitally controlled ICs: the TLV0834 and AD7801.

The T_x daughterboard consisted of the RGB LED driver circuitry [64].

For the R_x , the motherboard consisted of [65]:

- The digitally controlled ICs: the TLC5540, TXB0104 and PCM1744; and
- The audio output buffers and external audio RCA connectors.

The R_x daughterboard consisted of the colour detection circuitry [66].

The forethought in splitting the project layout in this manner was beneficial primarily for testing purposes. The colour transmission and detection circuits could be tested in isolation to the motherboards, and digital logic could be tested independent of the analog components.

The motherboards were constrained to 140mm in length and 100mm in width, while the daughterboards were constrained to 100mm in length and width.

The daughterboards attached to the motherboards via 90° pin headers. The pin headers served as power, ground and signal lines, as well as provided overall mechanical stability to the modules. Further stability to the modules was added by using two 160mm×160mm×3mm sized aluminium base plates to provide a counter balance to the 90° daughterboards (see Figure 39 and Figure 40).



Figure 39: T_x Construction

6.1 RGB LED Colour Array and Detector

The T_x daughterboard was carefully designed with respect to the viewing angle and projected optical emittance of the LEDs. The design is shown in Figure 41, varying slightly to the initial CAD design from Figure 7.

The R_x daughterboard was designed considering the radiance received from the T_x LEDs onto the projected solid area of the R_x was maximised (see Figure 42).

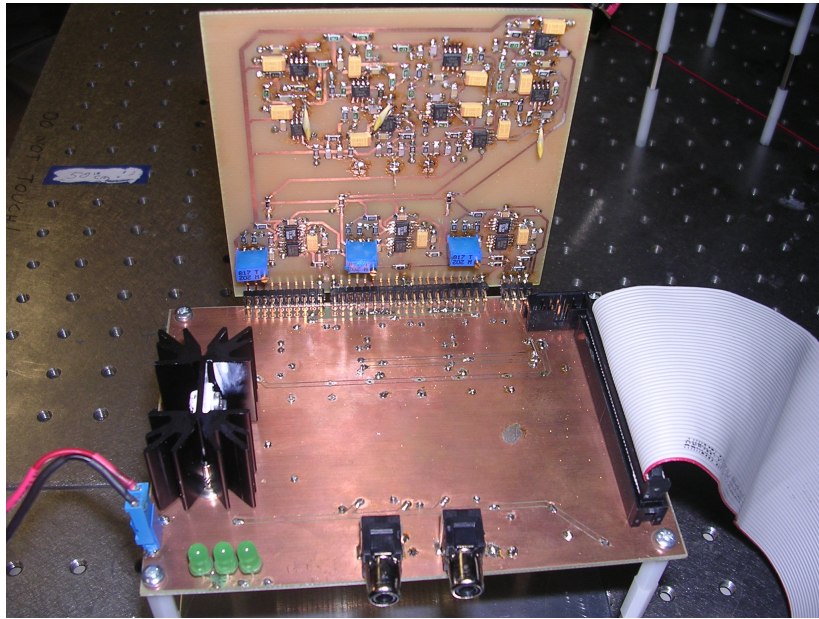


Figure 40: R_x Construction

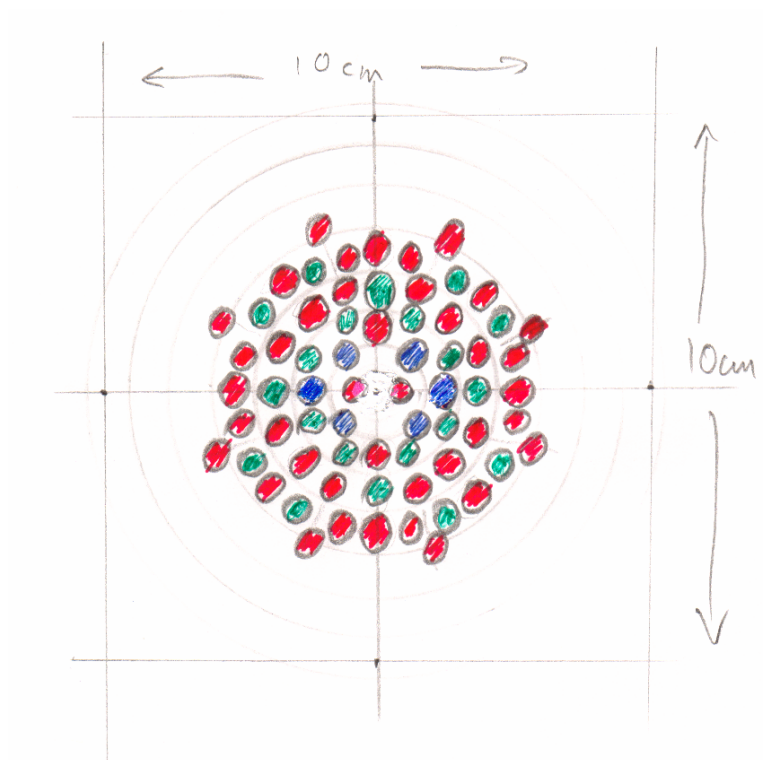


Figure 41: T_x RGB LED Array Configuration

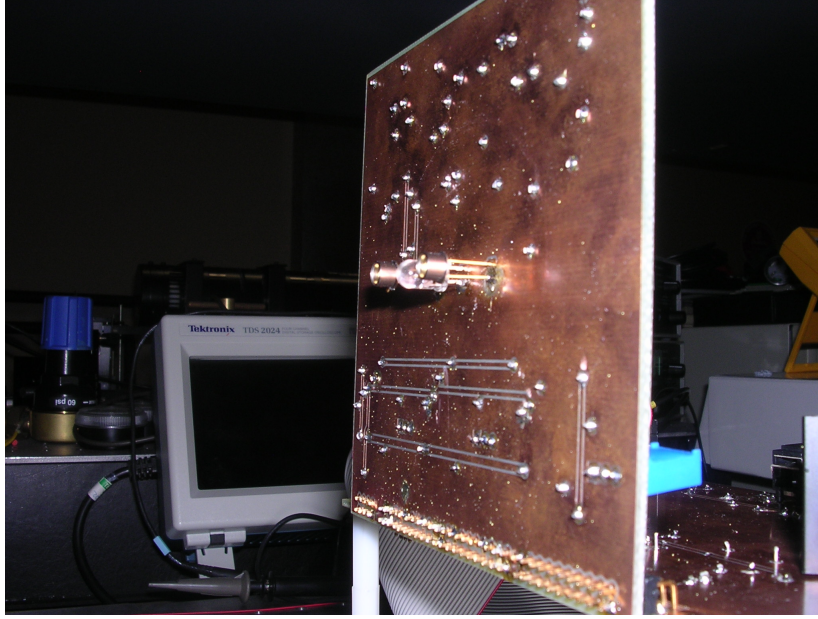


Figure 42: R_x Colour Detector Configuration

6.2 Thermal Consideration

The +5V regulators on each module required heatsinks to dissipate excess heat and prevent the regulators from going into thermal shutdown. The mechanical stability of the heatsinks and regulators was crucial as many devices required the +5V supply rail to function. To provide greater stability to the regulator on the T_x module and to distance the heatsink from any possible movement that could result in negative implications for the module electrical and functional stability, the heatsink and regulator were mounted horizontally (see Figure 43).

Mounting the T_x regulator and heatsink horizontally was not considered as a major loss with respect to vertical air flow due to the proximity of the control knob platform and T_x daughterboard to the regulator (see Figure 44). A bed of Araldite epoxy adhesive was used to provide mechanical stability to the heatsink and regulator and also as non-conductive buffer to the underlying +3.3V supply rail.

Araldite bond strength weakens above 65°C and begins to liquify at 150°C,

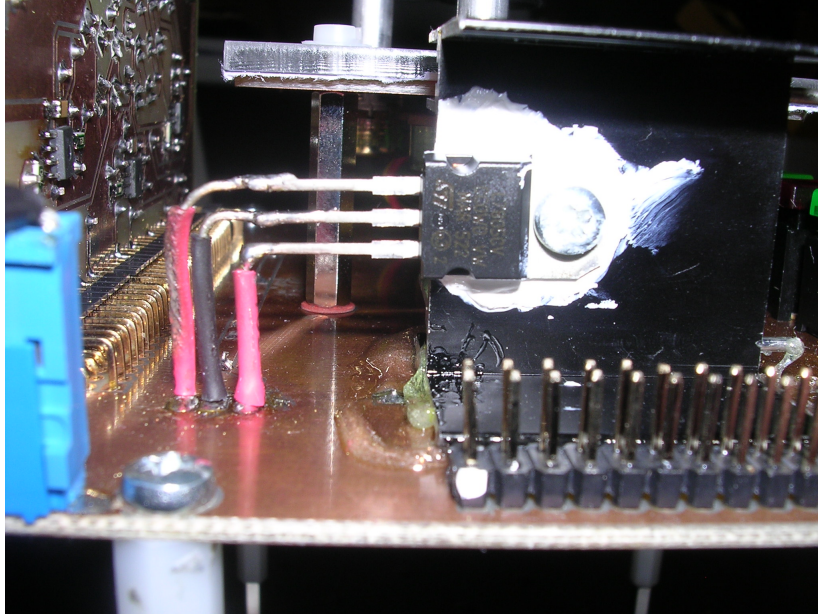


Figure 43: T_x Heatsink Horizontal Mounting

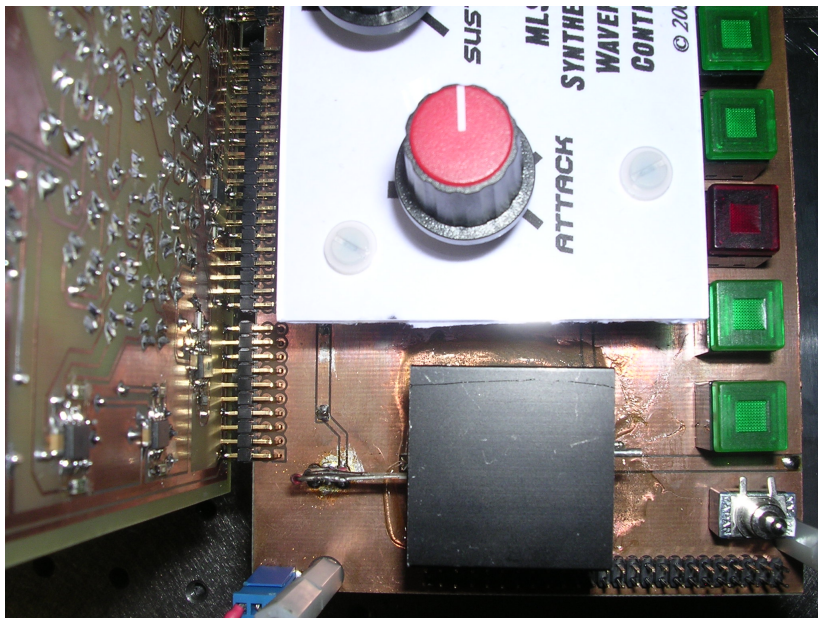


Figure 44: T_x Heatsink

but regains its strength if the temperature drops [67]. The expected heat dissipated from the $T_x + 5V$ regulator and heatsink is not expected to increase above $50^{\circ}C$ based on the vendor specifications and power budget calculated in Table 19. The R_x module's regulator and heatsink [59] were stabilised using the PCB and no special construction requirements were needed.

6.3 External Wiring

All external wiring connected to the modules was made via headers and connectors, enabling replacement parts to be easily interchangeable and connections to be robust (see Figure 45).

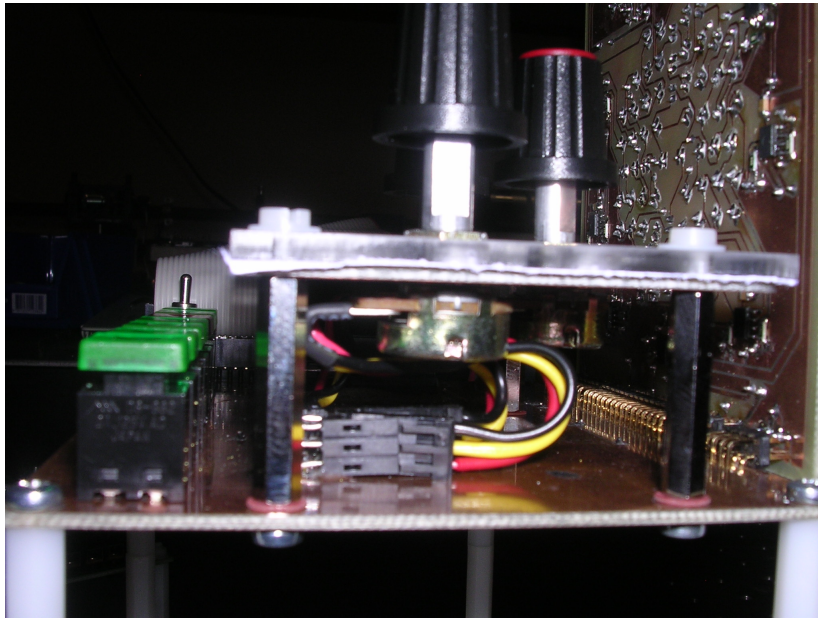


Figure 45: External Wiring

6.4 Summary

In this chapter, a comprehensive analysis of the physical considerations of the project design were presented and illustrated. The mechanical stability of the project was discussed in terms of connections between module motherboards

and daughterboards, heatsink and voltage regulators and external wiring attaching components to the project's modules. By providing a mechanically stable solution to the physical layout of the components, the probability of errors due to physical interconnections is decreased and hardware debugging made easier.

The construction of the board enabled the evaluation of the design, simulation and firmware components to begin. In the next chapter, the evaluation procedures and results for each component are presented.

7 Evaluation

The previous chapter described the physical layout and construction of the T_x and R_x modules of this project. The construction and manufacture of the modules provided the ability to begin taking measurements to confirm the system design and simulation.

In this chapter, we evaluate each component and describe the results of each evaluation, any issues that arose and how they were overcome.

7.1 Power

To test the power regulation of the T_x and R_x modules, load testing over a fifteen minute time period was used to establish the validity of choosing selected devices for +5V (L7805) and +3.3V (LM1117DT-3.3) regulation. Examples of the experimental setup for each module are displayed in Figure 46 and Figure 47.

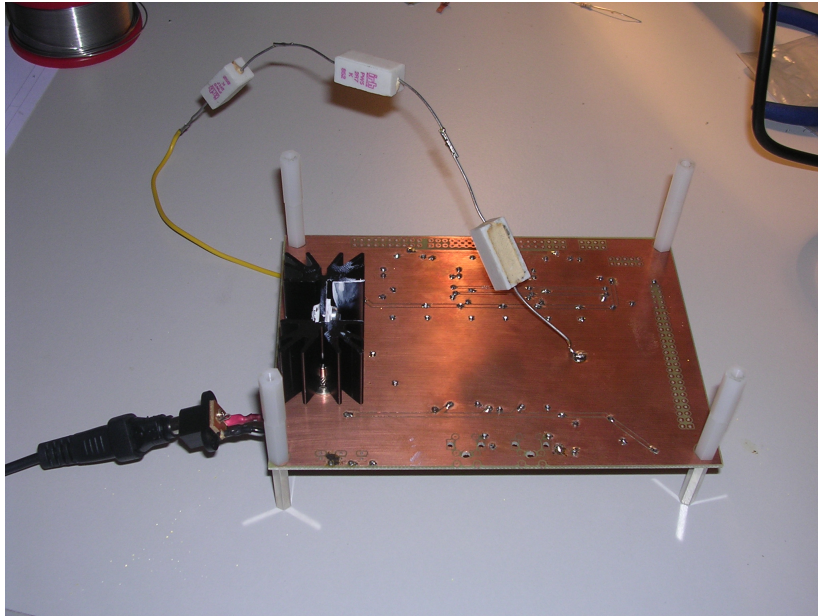


Figure 46: +5V Regulator Load Test Setup

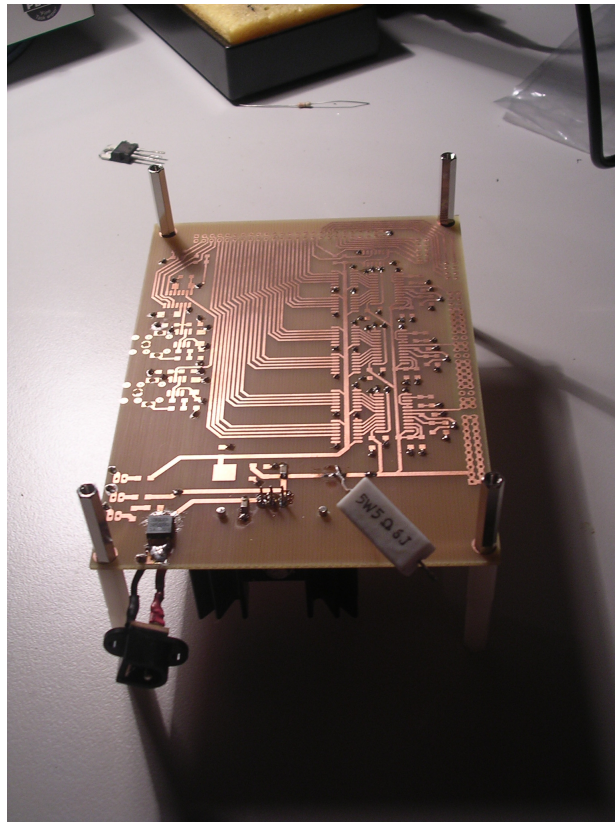


Figure 47: +3.3V Regulator Load Test Setup

The results of the tests (see Table 26 and Table 27) were similar for both modules. The heatsinks on the +5V regulators were sufficiently dissipating heat with a load current of 600mA; almost twice the load expected from the R_x module (see Table 20). The +3.3V regulators provided a stable voltage without dissipating a noticeable heat increase to the PCB when under a load current of 600mA; 600 times the expected load of the T_x module (see Table 19).

Time	V_a	V_b	V_c
10s	5.03V	3.37V	1.70V
45s	5.03V	3.37V	1.70V
90s	5.02V	3.36V	1.69V
180s	5.01V	3.37V	1.70V
300s	5.01V	3.37V	1.69V
600s	5.01V	3.36V	1.69V
900s	5.01V	3.36V	1.70V

Table 26: L7805 Load Testing

Time	V_{in}	+5V Rail
10s	3.27V	5.02V
45s	3.26V	5.02V
90s	3.26V	5.02V
180s	3.26V	5.02V
300s	3.26V	5.02V
600s	3.26V	5.02V
900s	3.26V	5.02V

Table 27: LM117DT-3.3 Load Testing

The voltage drop across the Schottky protection diode was tested to ensure that it was within the vendor specification and thus verified the choice of the particular diode in this design. The result of the voltage measurement proved conclusively that the diode was behaving as expected and suitable for the design. The result is shown in Table 28.

To provide electrical stability to both circuits, a 12V 5W Zener diode was added to the +12V supply rail to remove turn on transients and offer protection to the devices attached to the +12V rail [68, 69].

Module	V _{in}	V _{out}
T _x	12.28V	12.01V
R _x	12.01V	11.81V

Table 28: Schottky Diode Low Voltage Drop Test

7.2 User Input

The buttons and rocker switch were tested that the electrical response was correct when the button was depressed or rocker switch toggled. When the buttons or switch were toggled, the expected output was the voltage would raise to the +3.3V rail from GND. The tests for all buttons and rocker switches produced similar results to that shown in Figure 48.

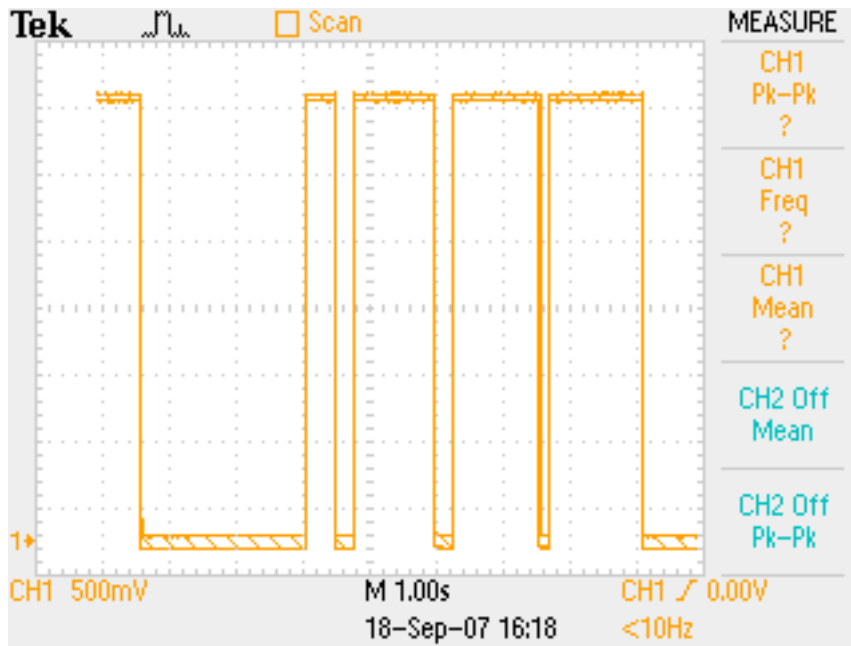


Figure 48: Electrical Button Debounce Test

When testing the firmware based debounce, no suspect activity was found on any key other than ‘Note G’, which was connected to the . The particular IO pin used by ‘Note G’ was the FX2_IO32 port on the S3EDK, and when pressed, the voltage would rise to +3.3V and continue to stay high, symbolising the IO line was being driven. The associated pin on the XC3S500E

Spartan-3E IC was ‘A11’. It was discovered that the ‘A11’ pin of the FPGA was shared with the MSB of the Intel StrataFlash address line on the S3EDK as well as the Xilinx Coolrunner-II CPLD on board the S3EDK.

Tests were carried out on the individual FX2_IO32 port’s input and output buffers internal to the FPGA by linking an unaffected button’s input to the affected port’s output buffer and vice-versa. The results of this test did not conclusively determine whether the input buffer on the affected port was damaged. Another attempt to solve this problem was to disable the FPGA pin, ‘C9’, controlling the CPLD; this did not rectify the issue. To resolve this issue quickly, the T_x ’s ADC SARS pin was disconnected from FX2_IO30 and a link was made to it from FX2_IO32. The ADC SARS output pin was a feature of the device to signal that conversion was taking place. The SARS pin was conveniently located next to the ‘Note G’ input pin, however this was not the primary reason for its choice. The particular functionality of the SARS pin was made redundant by the firmware communicating with the T_x ’s ADC, as it used validation techniques and timing associations to confirm conversion completion; thus the legacy IO line was able to be used for another purpose if so required [70, 71].

To resolve the issue with the ‘A11’ pin and any associated devices attached to it, firmware was written for the Coolrunner-II CPLD that consisted of an entity with one input and one output, and all other pins disabled.

7.3 Transmitter DAC

The verification of the transmitter DACs used ramp and saw generator code to supply 8-bit words to generate the resultant expected output of these common waveforms. Figure 49 and Figure 50 show the resultant output of the DACs. The output of Figure 49 matches the simulated version from Figure 31, thus confirming that the digital device timing criteria has been satisfied for these devices and that they perform as expected.

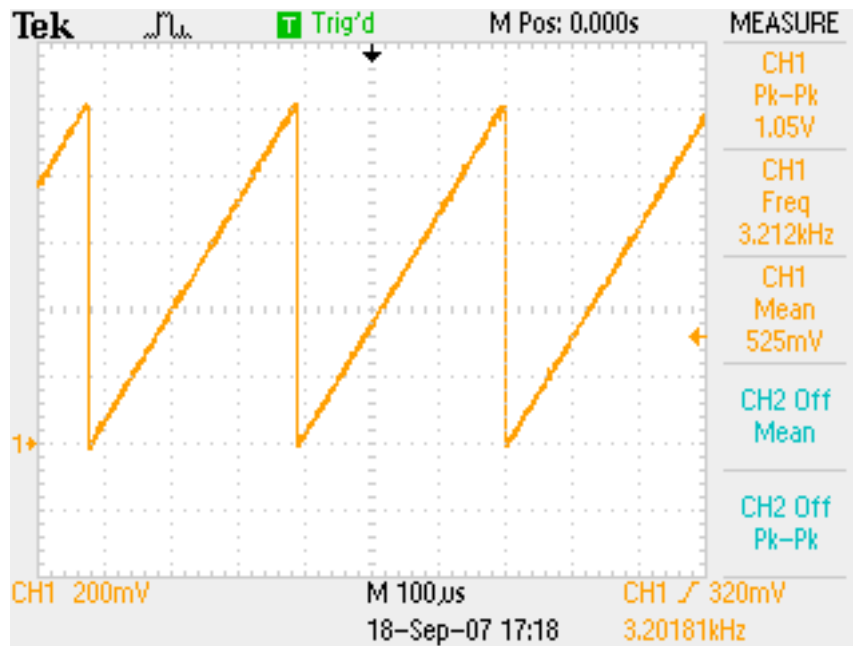


Figure 49: T_x DAC Test - RAMP Generator

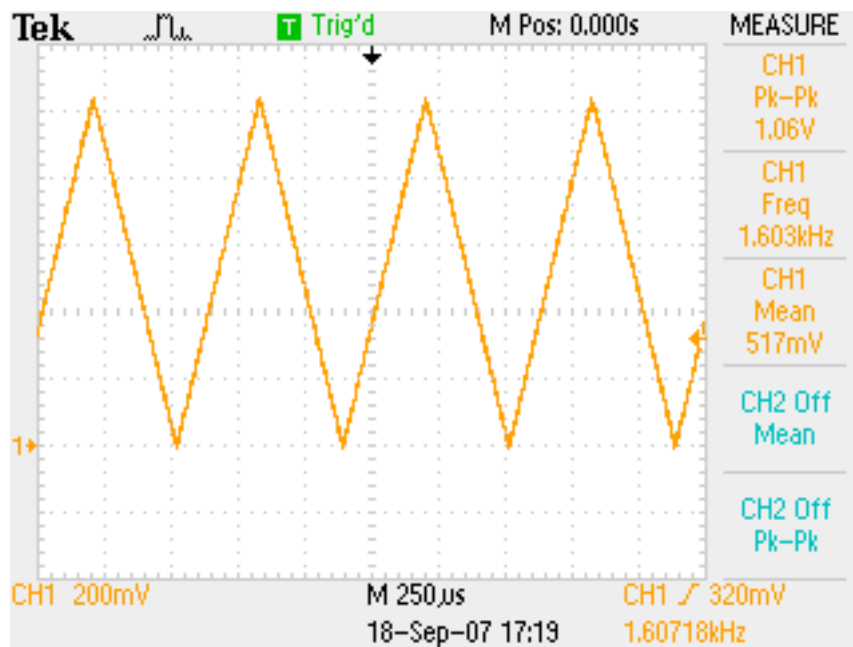


Figure 50: T_x DAC Test - SAW Generator

7.4 Control Knobs and Transmitter ADC

To test each of the control knobs and the associated ADC functionality, the 8-bit ADC output was routed to the parallel 8-bit DAC on the T_x module. A multimeter was used to measure the voltage at the wiper of the potentiometer, with the output of the DAC used to confirm that the correct voltage was translated to an 8-bit digital word.

Test Voltage	Attack Knob		Sustain Knob		Decay Knob	
	Multimeter	CRO	Multimeter	CRO	Multimeter	CRO
0V	0V	0V	0V	0V	0V	0V
1.65V	1.65V	2.53V	1.65V	2.53V	1.66V	2.55V
2.50V	2.50V	3.84V	2.50V	3.86V	2.50V	3.86V
3.30V	3.29V	5.01V	3.29V	5.01V	3.29V	5.01V

Table 29: Control Knob and T_x ADC Testing

From the results in Table 29 a ratio test of the DAC output, the results confirm the ADC is correctly converting the analog signal produced by the rotation of the potentiometers. The minor discrepancies in the ratio test (see Table 30) are tolerable for the functionality required of the control knobs in this design (attributed to the compound error in conversion between the ADC and DAC). Evaluation of the control knobs via the ADC and DAC verified that the ADC conversion process is functional, thus meeting the digital timing requirements of the vendor specification.

Test Voltage	Attack Knob		Sustain Knob		Decay Knob	
	+3.3V	+5.0 V	+3.3V	+5.0 V	+3.3V	+5.0 V
0V	0	0	0	0	0	0
1.65V	0.50	0.50	0.50	0.51	0.50	0.51
2.50V	0.75	0.76	0.75	0.77	0.75	0.77
3.30V	0.99	1.0	0.99	1.0	0.99	1.0

Table 30: T_x ADC and DAC Ratio Relationship

7.5 Digital Potentiometers

To enable the use of the filter circuits with digital control, the timing diagrams were verified for each of the RGB associated digital potentiometers. The timing results for all devices matched those simulated in Chapter 5. Figure 51 presents the result of loading the 8-bit word 68_{16} onto the SDI pin of the device.

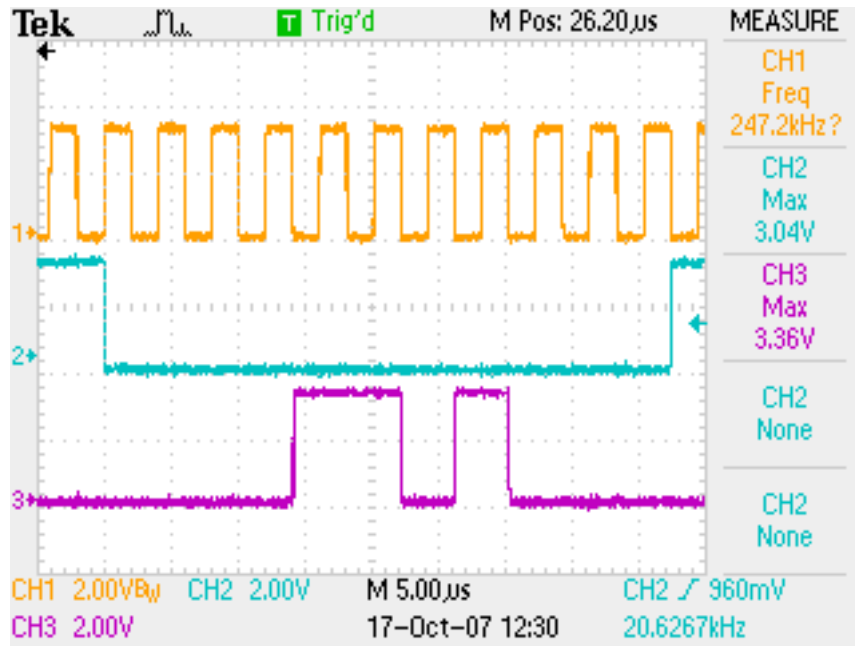


Figure 51: Digital Pot Timing Confirmation for the Green filter. Channel 1 is the digital potentiometer CLK signal, Channel 2 is the $\overline{CS}$ signal and Channel 3 is the 10-bit data word used to load the step resistance.

As all timings were confirmed, the digital potentiometer steps sizes were loaded such that the resultant filter output would be a $2V_{pp}$ signal received from the T_x LED array. Values measured from using standard linear potentiometers to achieve a $2V_{pp}$ signal were used as a reference for setting the digital equivalent step size. The input signal for this experiment from the T_x LED array was a $1V_{pp}$ 50kHz sinusoidal wave.

The test results (from Table 31) show that the digital potentiometer resistance values used to obtain a $2V_{pp}$ are similar to those used by the linear

potentiometers. Device specific impurities, reliability of measuring equipment and temperature drift are factors for the resultant differences. The digital potentiometer values were successful in being able to linearly adjust the resultant input voltage from the filter circuits (see Figure 52).

Filter	Potentiometer Type		Digital Step Size	
	Linear	Digital	Expected	Actual
Red	263 Ω	206.2500 Ω	4 - 04 ₁₆	$\odot$
		245.3125 Ω	5 - 05 ₁₆	
		285.3750 Ω	6 - 06 ₁₆	
Green	4.05k Ω	4034.3750 Ω	102 - 66 ₁₆	$\odot$
		4073.4375 Ω	103 - 67 ₁₆	
		4112.5000 Ω	104 - 68 ₁₆	
Blue	1.845k Ω	1768.7500 Ω	44 - 29 ₁₆	$\odot$
		1807.8125 Ω	45 - 2D ₁₆	
		1846.8750 Ω	46 - 2E ₁₆	

Table 31: Digital Potentiometer 2V_{pp} Calibration

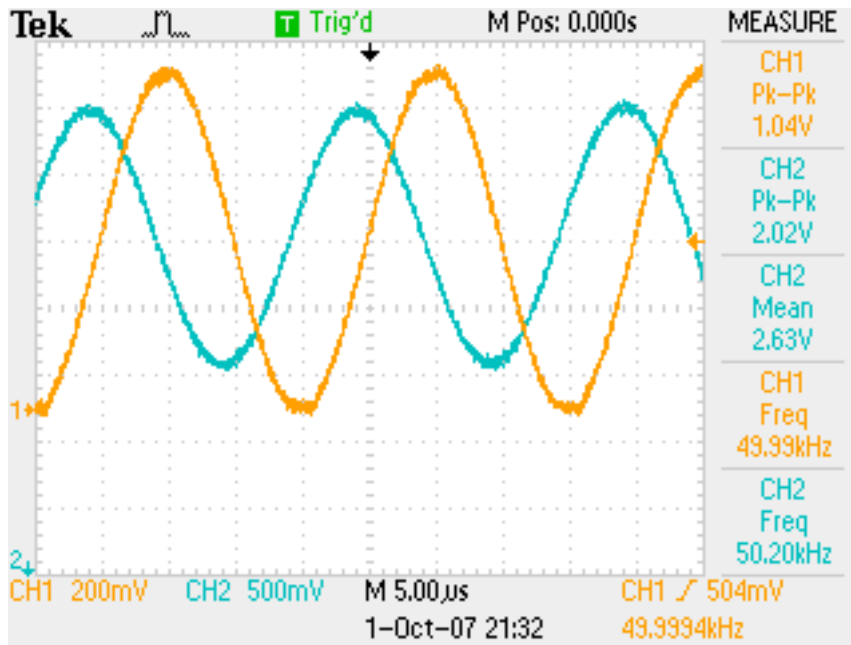


Figure 52: Digital Potentiometer Linear Gain Adjustment. Channel 1 is the transmitted light and Channel 2 is the VGA resultant output signal.

7.6 Waveform Detector and Receiver ADC

The combinatorial evaluation of the waveform detector and receiver ADC encountered a severe problem with the supporting devices that translated the logic voltage levels between the FPGA and the ADC. The CLK signal sent to the ADC was unable to be translated by the TXB0104. Several versions of the image shown in Figure 53, were able to be translated to +3.9V, but did not reach the minimum voltage required for the ADC, $V_{IH}=4V$.

Adding decoupling capacitors to the device did not resolve the issue (see Figure 54), however it removed some of the noise present in the CLK signal. The input CLK frequency was scaled from 1MHz - 12.5MHz, with the same result. The physical layout of the device was scrutinised, the vendor specifications re-assessed and devices replaced. The bi-directional logic translators did not function as specified, or the devices shipped from the manufacturer were damaged by ESD. Unfortunately, the cause of the fault was not discovered, however, a resolution to the problem was found.

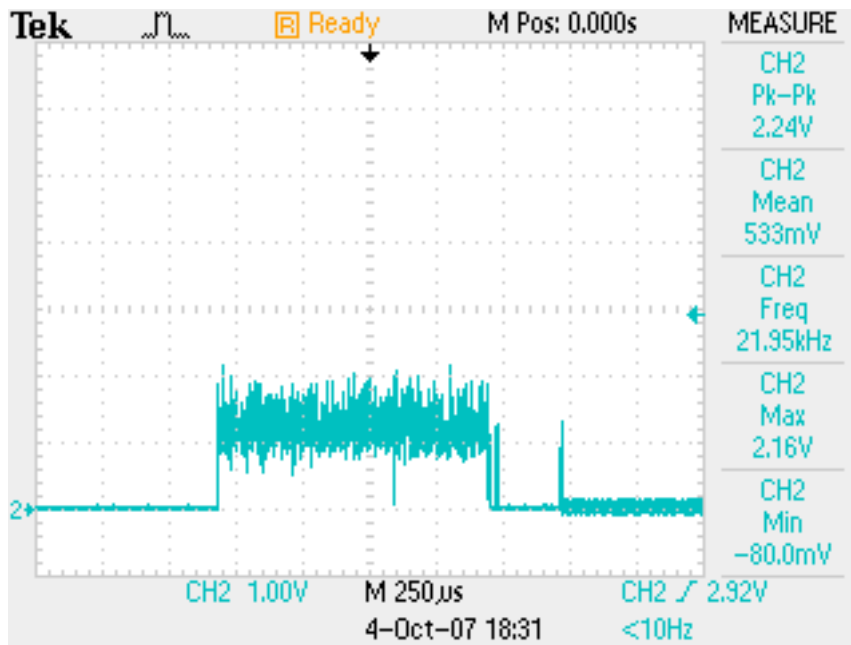


Figure 53: Voltage translator output signal not being translated.

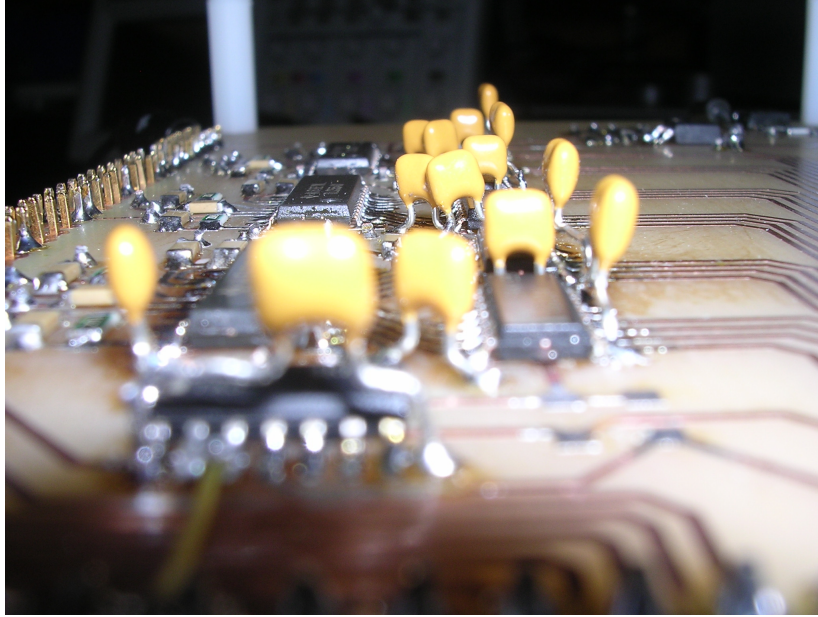


Figure 54: Adding decoupling capacitors to the voltage translators did not solve the problem.

To resolve the logic translation problem, a switching transistor was used to provide the logic translation for the ADC CLK signal, while the ADC $\overline{\text{OE}}$ was tied to GND. The switching transistor solution would invert the CLK signal: a logic low would turn the transistor off, resulting in a logic high for the ADC; while a logic high would turn on the transistor, resulting in a logic low for the ADC [72]. A firmware solution was used to invert the CLK signal to the ADC before being sent out of the FPGA, thus negating this effect. To overcome the logic translation from the output of the DAC, the outputs used a voltage divider to scale the voltage from +5V to +3.3V [72, 73, 74] (see Figure 55). Although the desirable outcome was achieved using this solution, the maximum rate that the transistor could switch was 2.5MBPS, at which point Miller effects would degrade the signal.

After resolving the logic translation issue, the waveform detector and R_x ADC were tested for correct functionality. The timing of the ADC was verified (as shown in Figure 56) against the vendor specifications and was found to be correct, both in simulation and implementation.

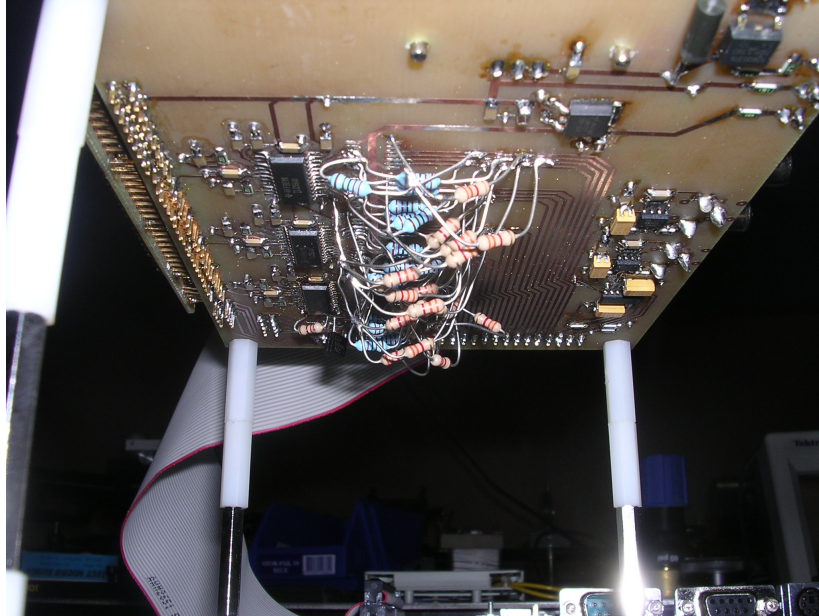


Figure 55: Solving the logic translation issue with a switching transistor and resistor dividers.

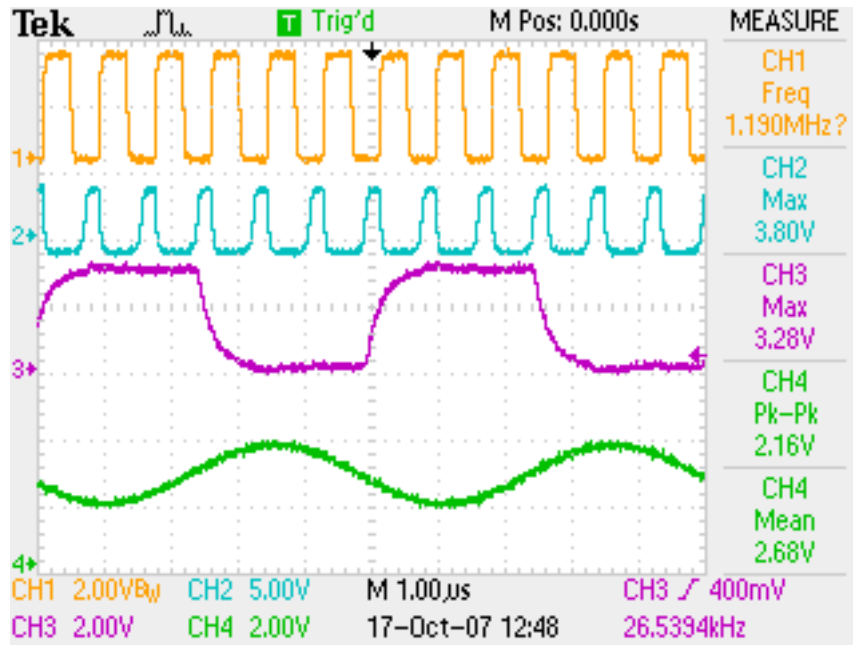


Figure 56: R_x ADC Timing Verification. Channel 1 is CLK, Channel 2 is transistor output, Channel 3 is MSB of the ADC, Channel 4 is a sinusoidal input signal.

Testing of the waveform detector was made possible due to the reconfiguration of the R_x motherboard. As the ADC $\overline{OE}$ pin was no longer used, it was possible to use it as a test pin. Pulses were sent from FPGA to the test pin to confirm the correct operation of the waveform detector. When a peak greater than 3V was detected, a logic high was set, otherwise a logic low would be set. The output waveform, Figure 57, confirms the waveform detector was functioning correctly.

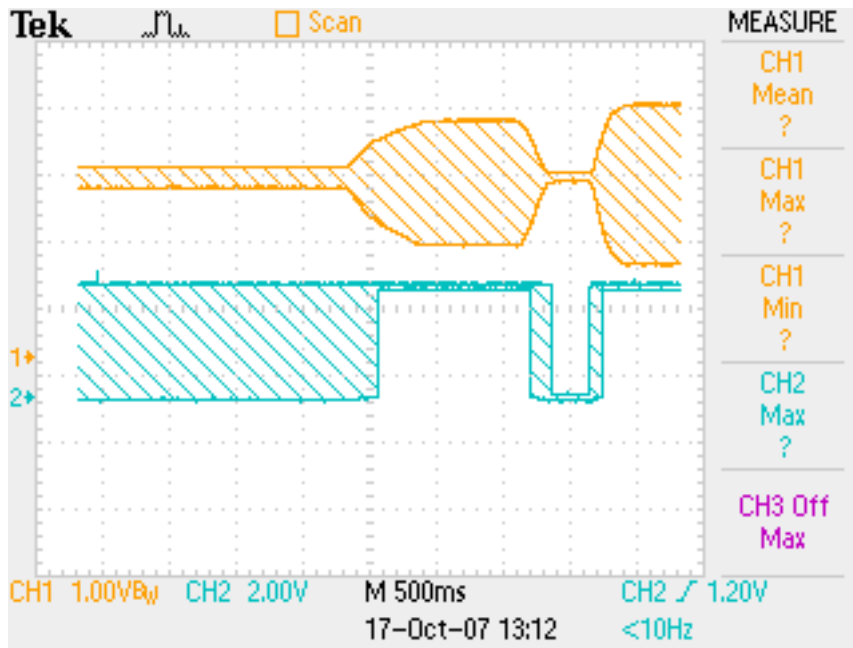


Figure 57: R_x Waveform Detection. Channel 1 is the input sine wave, Channel 2 is the peak detection pulse (Logic High if Channel 1 > 3V).

7.7 Numerical Controlled Oscillator and Audio DAC

The evaluation of the R_x module's audio DAC and NCO algorithm occurred in parallel. The NCO output was the input bitstream for the audio DAC's conversion word. The generated output of the NCO produced a periodic waveform that could be adjusted according to the tuning word used to begin audio generation. Figure 58 and Figure 59 present the results of two exper-

iments that were conducted to verify the correct operation of the DAC and that of the NCO.

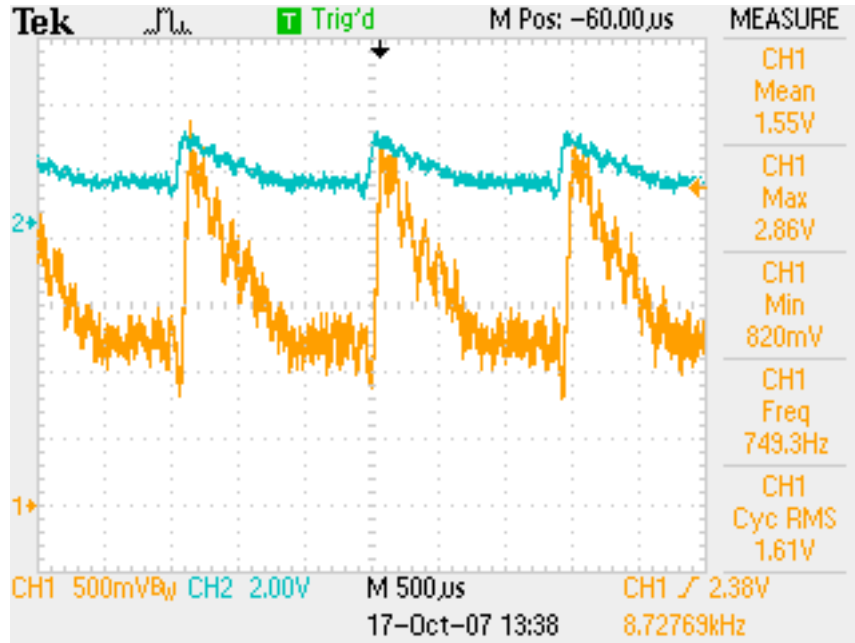


Figure 58: Periodic NCO from DAC– Tuning Word of 220. Channel 1 is the left channel output, Channel 2 is the right channel output

The results verified that the audio dac firmware complied with the Phillips I²S input format and was able to produce audible sound. The NCO output was not intended to produce the waveform generated, however, the periodic nature of the waveform does not suggest that timing is causing the unexpected output. The areas of interest for analysing the erroneous logic flow are in the NCO components governing the virtual memory-to-physical memory mapping, in the NCO adder and the logic controlling the extraction of values from the block RAM. Pipelining of arithmetic or wrongly inserted data into the block RAM could be contributing factors to this waveform.

The unexpected waveform shape did produce a unique sound, with adjustable frequencies based on different tuning words used as the input to the NCO. The resultant waveform produced by the DAC is audible and quite unique.

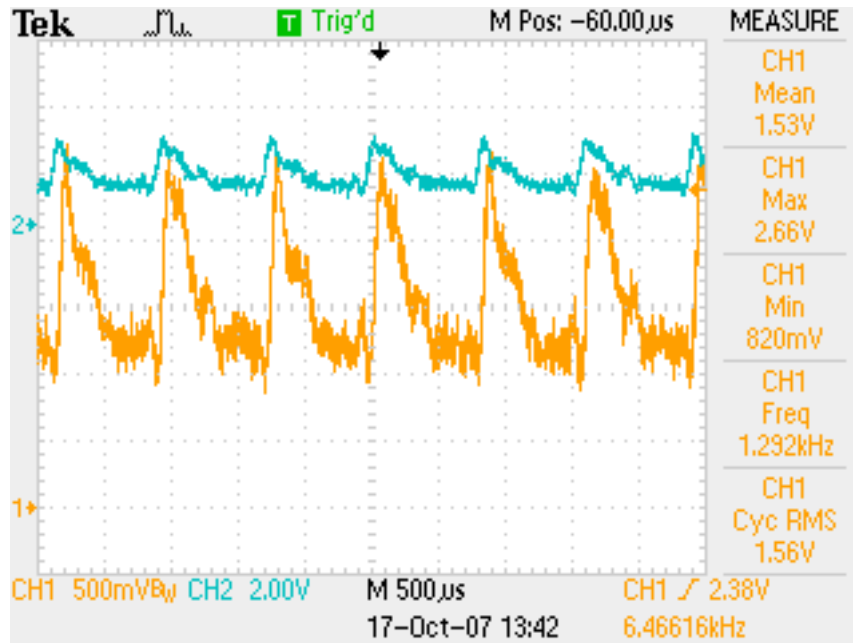


Figure 59: Periodic NCO from DAC – Tuning Word of 392. Channel 1 is the left channel output, Channel 2 is the right channel output

7.8 Audio Output

The audio output buffers were tested to confirm the analog operation of the opamps. Varied frequencies in the audible range of 20Hz – 20kHz, were used as an input to the left and right channel audio buffers. The expected results of opamps was an +2.5V DC biased signal with a peak-to-peak voltage equivalent to the input signal (see Figure 60). Phase alignment was negligible between the input and output signals as expected (see Figure 61).

The results of these experiments demonstrated that the audio output buffers would successfully be able to buffer the audio generated by the R_x 's audio DAC.

7.9 Filter Response

To scrutinise the filter response, the TINA PSpice simulation from Chapter 5 was tested. Constant current sources were created through series and parallel

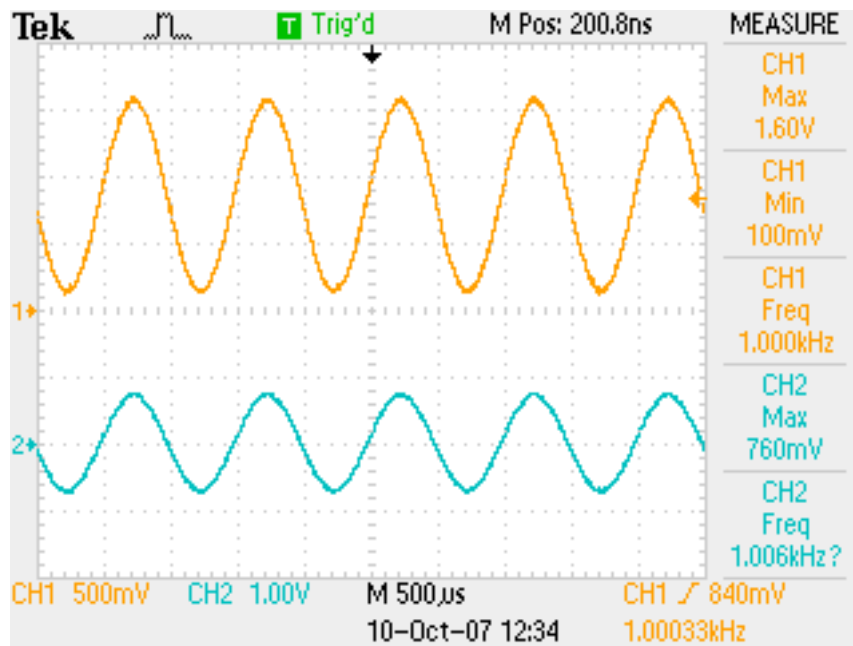


Figure 60: Audio Output Buffer Signal Test. Channel 1 is the input frequency, Channel 2 is the DC biased output of the opamp.

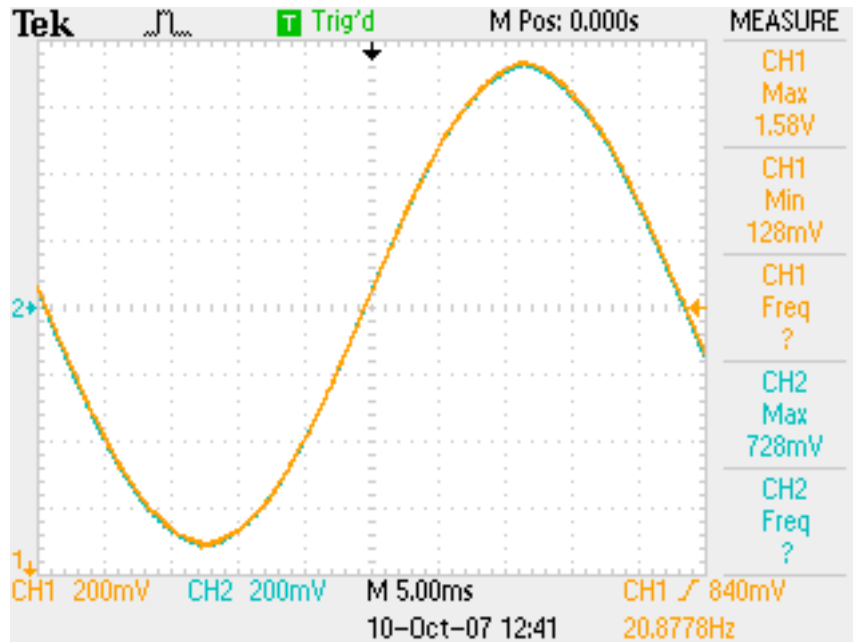


Figure 61: Audio Output Buffer Phase Test. Channel 1 is the input frequency, Channel 2 is the DC biased output of the opamp. Phase differences between the two signals is marginal.

resistor combinations as shown in Figure 62. The experiment only focused on the output stage of the filters (N5 from the TINA PSPice simulation), with linear potentiometers used in place of their digital equivalent. The results in Table 32 present significant differences between the expected resistor feedback values and those actually measured.

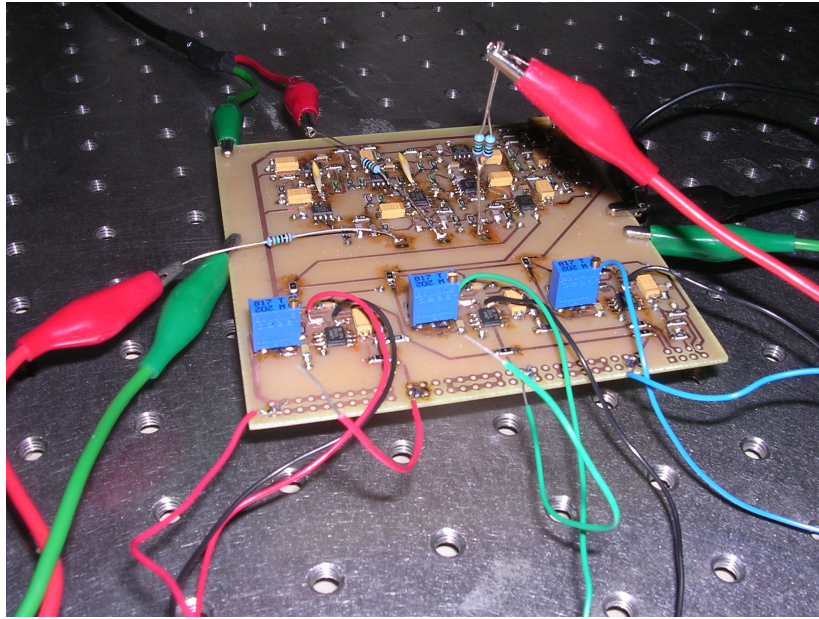


Figure 62: Nodal Voltage Testing on N5

Filter	Input Current	Resistance		Measure Voltage	
		Simulated	Actual	DC Level	Amplitude
Red	$I_{\min}=250\text{nA}$	3487.5000Ω	$1.151\text{k}\Omega$	2.52V	2.02V
	$I_{\min}=1.1\mu\text{A}$	401.5625Ω	293.00Ω	2.51V	2.00V
Green	$I_{\min}=250\text{nA}$	3487.5000Ω	$2.38\text{k}\Omega$	2.51V	2.00V
	$I_{\min}=1.2\mu\text{A}$	323.4375Ω	190.00Ω	2.50V	2.02V
Blue	$I_{\min}=1.0\mu\text{A}$	2510.9375Ω	$2.05\text{k}\Omega$	2.48V	2.01V
	$I_{\min}=4.5\mu\text{A}$	167.1875Ω	95.5Ω	2.50V	2.03V

Table 32: Nodal Voltage Test for TINA PSPice Node Point N5

To evaluate and confirm that the filter circuits were sufficiently AC coupled, each filter circuit was tested against a range of frequencies from 50Hz to 100kHz. With an input sine wave of $1V_{pp}$ and linear potentiometers calibrated to produce a $2V_{pp}$ output at 50kHz, frequencies under 2kHz produced an 80mV response from the RGB filters. The graph presented in Figure 63 describes the frequency vs normalised amplitude response from all three filter circuits. The result of this experiment confirmed that the filter circuits were sufficiently AC coupled, such that daylight and ambient light would not impact on the ability for the R_x to discriminate between colour information.

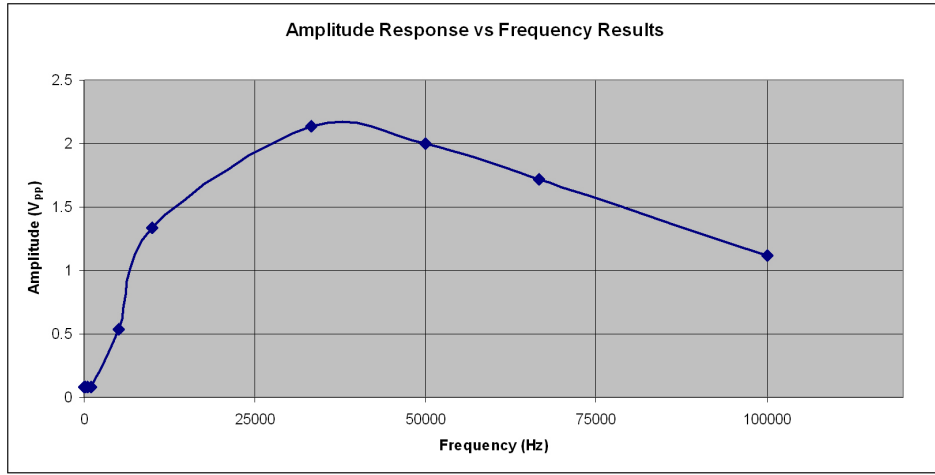


Figure 63: Amplitude Response Results

7.10 Colour Transmission and Detection

As a result of the modular implementation of the project's PCBs, the T_x and R_x daughterboards were able to be evaluated concurrently. The experiments were conducted by driving the T_x LEDs with a 50kHz sinusoidal signal with an amplitude of $1V_{pp}$ (see Figure 64) and having the R_x situated 54cm directly opposite the T_x . Linear potentiometers in the R_x VGA section were used in place of the digital potentiometers. The evaluation procedures for colour transmission and detection were based on the construction of a colour matrix, similar to that of Table 33. The inverse representation of the colour

matrix, ie, the associated currents of the T_x LEDs was the primary goal behind these experiments.

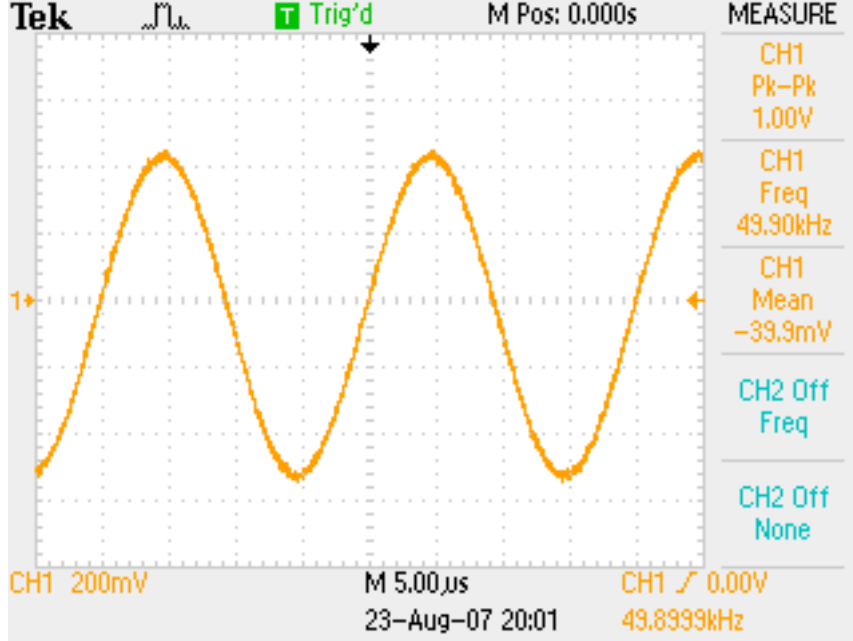


Figure 64: Drive Signal for T_x LEDs, a 50kHz sinusoidal signal with an amplitude of $1V_{pp}$.

R_x	T_x		
	Red	Green	Blue
Red (V)	$2V_{pp}$	$424mV_{pp}$	$368mV_{pp}$
R_F	400Ω	$9.79k\Omega$	$9.19k\Omega$
Green (V)	$560mV_{pp}$	$2V_{pp}$	$640mV_{pp}$
R_F	$9.47k\Omega$	$9.46k\Omega$	$9.46k\Omega$
Blue (V)	$1.5V_{pp}$	$800mV_{pp}$	$880mV_{pp}$
R_F	$10.06k\Omega$	$10.02k\Omega$	$10.06k\Omega$

Table 33: T_x / R_x Colour Matrix. Initial test results using the matrix.

Table 33 did not keep the value fixed for R_F , thus making a direct comparison using these results was inappropriate. However, these results did indicate that the intensity of the red T_x LEDs could be reduced by 20% (see Figure 65), and the green T_x LEDs by 70%. This resulted in better colour discrimination by directly affecting the detected voltage at each detector.



Figure 65: Initial Colour Transmission

R_x	T_x		
	Red	Green	Blue
Red (V) R_F	$2V_{pp}$ 777Ω	$112mV_{pp}$ 770Ω	$152mV_{pp}$ 780Ω
Green (V) R_F	$620mV_{pp}$ $8.56k\Omega$	$2V_{pp}$ $8.54k\Omega$	$820mV_{pp}$ $8.54k\Omega$
Blue (V) R_F	$420mV_{pp}$ $9k\Omega$	$980mV_{pp}$ $9k\Omega$	$1.04V_{pp}$ $9k\Omega$

Table 34: T_x / R_x Colour Matrix. $I_{RED}=19.6mA$, $I_{GREEN}=23mA$

The results from Table 34 could be directly compared, as the R_F of the VGA was fixed to the same value for all test cases with respect to each filter. The results from this experiment suggested two primary areas of concern, that the gain of the green and blue filter circuits was not large enough, as the VGA was near its maximum, and that the green and blue T_x LEDs were not bright enough.

After making modifications to the green and blue filter circuits [75, 76], more matrix experiments were conducted to find the resultant inverse current ratios. Through testing, it was established that the relationship between the filter circuits and initial set of T_x LEDs would not produce an effective colour discrimination. A modification to the green and blue T_x LEDs attempted to use the fringe wavelength frequencies supported by the green and blue photodiodes respectively (refer to Figure 3 and Figure 4), to produce more distinct differences between the colour detection of the green and blue transmitted light.

The new T_x LEDs had dominant peak wavelengths of 570nm and 435nm for the green and blue respectively, with each having tight spectral widths for LEDs [77]. The new LED drive currents were maximised to just over safe operating ratings of 30mA to 33.33mA, ie, with current feedback resistor values of 30Ω [78].

The effect of the 435nm blue LED was very promising (see Figure 67 and Figure 68), however the 570nm green LEDs (see Figure 66), were not detected by the green filter circuit at all, contrary to the photodiode datasheet specification. The only signal produced was the amplification of the ‘noise floor’ of the opamp.

Another set of green LEDs was acquired for use in experimentation and their results in colour discrimination tests was better than previous LEDs. In structuring subsequent tests, a more pragmatic empirical approach was taken; ie, understanding that there will be no perfect matrix and that firmware could be used to discriminate the received colours at a finer bit level. The daughterboards were attached to their respective motherboards and the T_x module was programmed to output 1V, 750mV and 500mV driving voltages

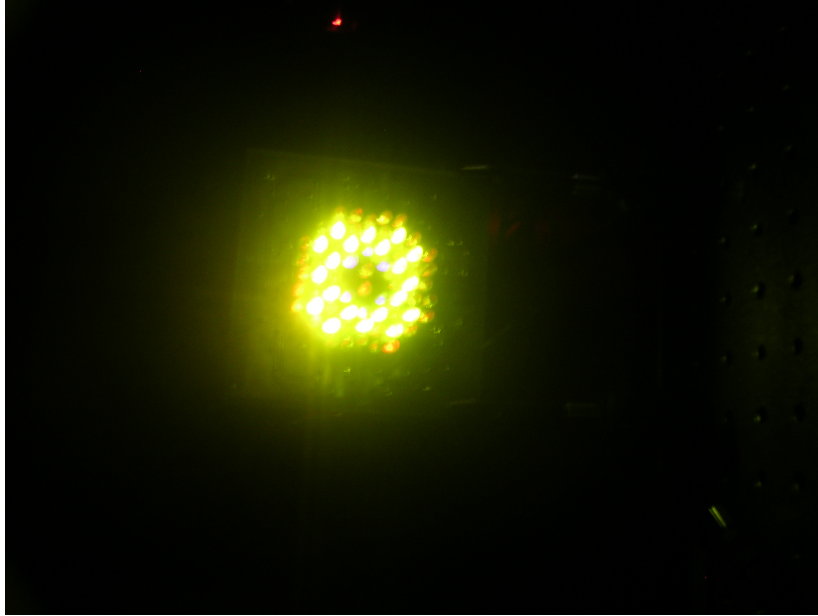


Figure 66: 570nm Transmission LEDs in place of the Green 525nm LEDs

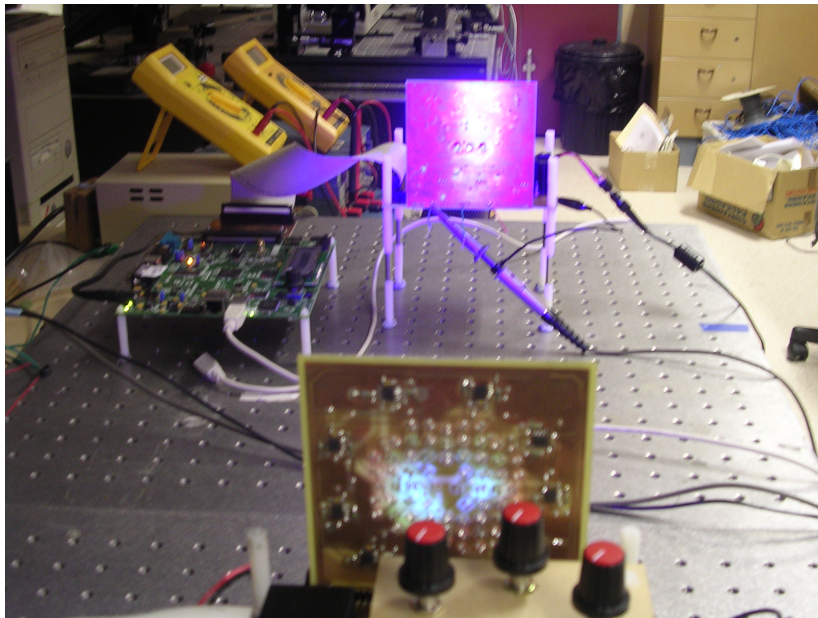


Figure 67: T_x Viewpoint of R_x

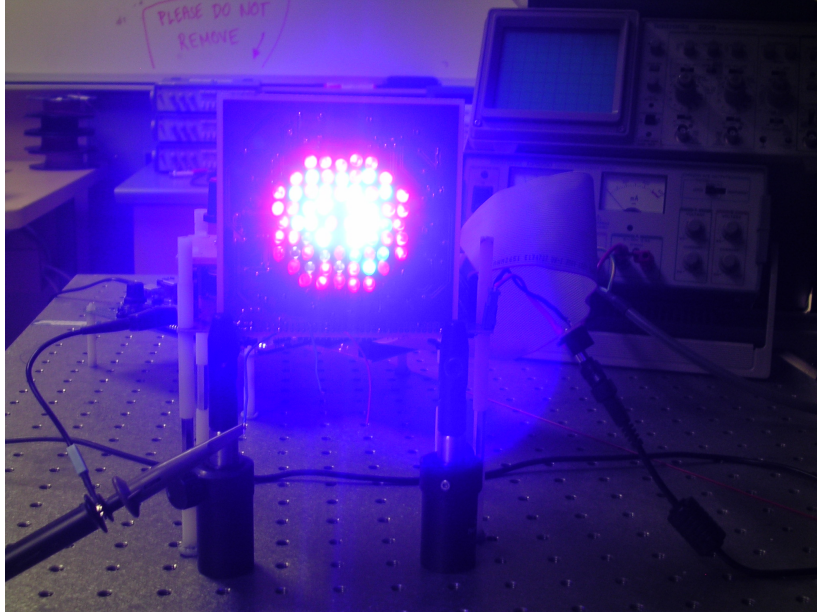


Figure 68: R_x Viewpoint of T_x

for the LED circuitry, while the R_x FPGA configured the digital potentiometers to the values discussed earlier.

Key	T_x			R_x		
	Red	Green	Blue	Red	Green	Blue
A	1V	-	-	$2V_{pp}$	$440mV_{pp}$	$1V_{pp}$
B	-	-	1V	$80mV_{pp}$	$440mV_{pp}$	$2V_{pp}$
C	0.75V	0.5V	-	$1.52V_{pp}$	$1.35V_{pp}$	$1.05V_{pp}$
D	0.75V	-	-	$1.52V_{pp}$	$440mV_{pp}$	$800mV_{pp}$
E	-	0.5V	-	$80mV_{pp}$	$1.25V_{pp}$	$400mV_{pp}$
F	0.5V	-	-	$1.02V_{pp}$	$440mV_{pp}$	$560mV_{pp}$
G	-	1V	-	$80mV_{pp}$	$1.82V_{pp}$	$620mV_{pp}$

Table 35: T_x / R_x Colour/Key Mapping

As a result of running more experiments, Table 35 was measured as the optimal colour transmission to detection mapping matrix. These values were used to create the driving logic that discriminates these voltages within the FPGA, allowing the system to be tested as a whole.

7.11 System Function

As a modular approach to implementation was used, the system functionality was implemented and tested with each design component. The overall system function was to synthesise an audible tone from the discrimination of received colour at the receiver from the transmitted colour generated by a user key press. To produce this system functionality, the system components were integrated and tested, with the T_x and R_x at a distance of 54cm opposite each other. The experiment used four locations on the project for testing, they were:

1. At the T_x keys;
2. At the output of the T_x DAC;
3. At the input to the R_x ADC; and
4. At the R_x RCA connectors

The results of these experiments confirmed that the project was able to synthesise an audible tone from the discrimination of received colour at the receiver from the transmitted colour generated by a user key press. The output waveforms of the tests are shown in Figure 69 and Figure 70.

The analysis of the waveform results show that:

- There is $150\mu s$ delay between user key press and transmission;
- There is negligible delay between transmitting and receiving light; and
- There is $700\mu s$ delay between discrimination the received light and producing an audible tone.

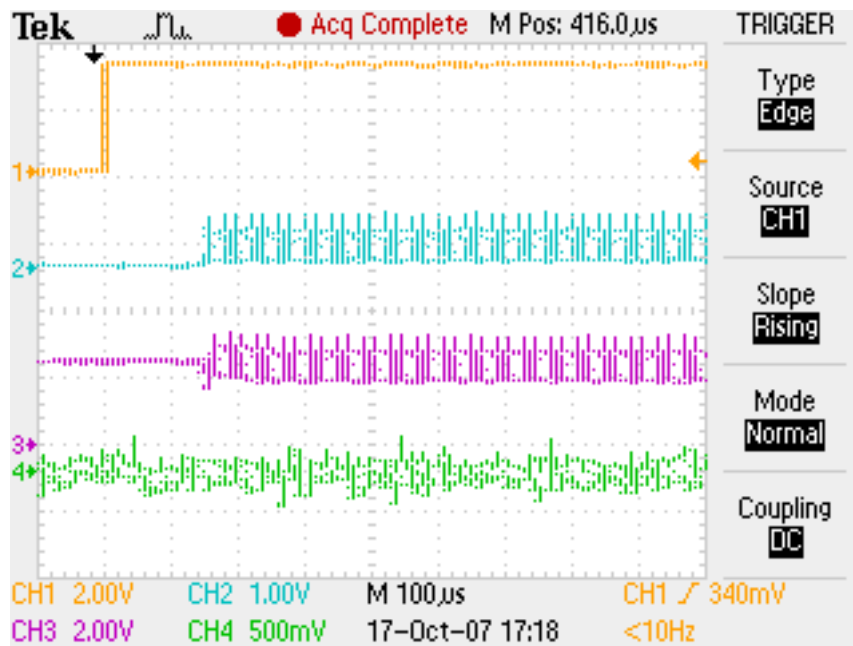


Figure 69: End to End System Test. Channel 1 - User Key, Channel 2 - T_x DAC, Channel 3 - R_x ADC, Channel 4 - Output RCA

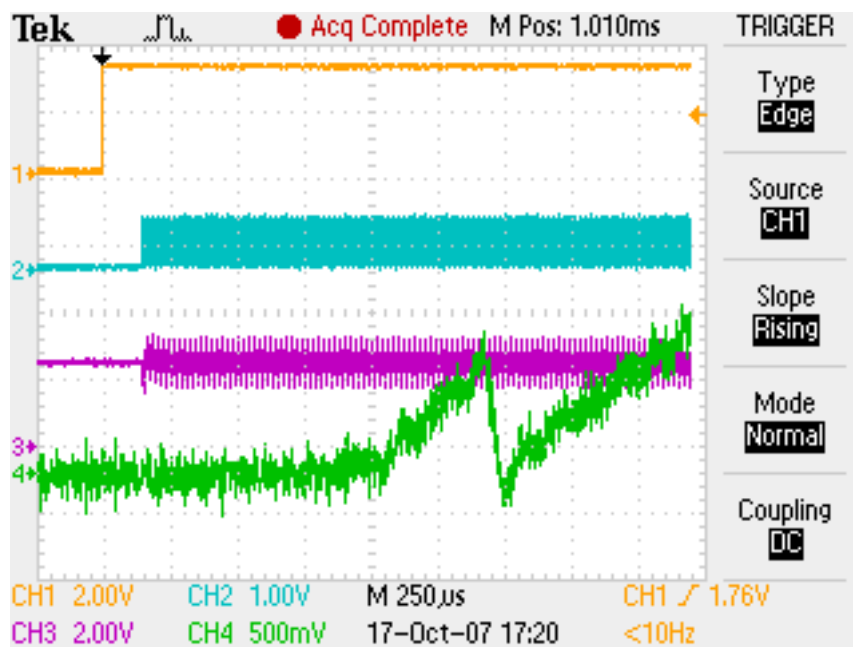


Figure 70: End to End System Test. Channel 1 - User Key, Channel 2 - T_x DAC, Channel 3 - R_x ADC, Channel 4 - Output RCA

7.12 Summary

This chapter presented the results of the experiments used to verify and corroborate the design and simulation of this project. Each design and simulation component was evaluated to ensure vendor specifications were accurate, functional implementations were accurate, as well as to modularise the design so errors could be rectified if present. Some experiments came across issues which needed to be resolved before verification of components could be assessed. Solutions were found and tests carried out to rectify these issues.

All the experiments in this chapter successfully validated the system design from Chapter 4 and the simulation procedures in Chapter 5. The resultant system function test was successful in producing a result that brought together each component that was evaluated in this chapter. In the next chapter, we discuss our findings with respect to our critical project objectives and discuss future work.

8 Conclusion

“Music is the movement of sound to reach the soul”

– Plato

In the beginning there was light.

What followed was a sound.

Then an idea.

“If light could be used to produce sound, could we control this light in such a manner that we could produce controlled audible sounds?”

In this project we have answered the question with an emphatic “Yes!” What started as a novel idea for forging the visual senses with the aural, developed into a set of key criteria, the critical project objectives. The objectives were formed into a series of experiments to demonstrate the plausibility of creating something that could use visible light to control sound. The results of the feasibility experiments resulted in a broad description of a model for design, simulation, construction and evaluation.

The critical project objectives were used as a reference for the systematic design of all components described by the analysis of the feasibility experiments. The design included the logic control, the user interface, the conversion of analog and digital data, the audio output requirements, the power considerations and most importantly a thorough inspection of the transmission and detection circuitry.

To gain more confidence in the design, simulations were performed on the analog detection circuitry and the firmware. Simulations aided in the verification of design decisions and were used when evaluating the physical implementation as a baseline reference. Construction of the board provided

a thorough mechanical base for the project, lessening the impact that problems caused by the physical layout and positioning of components would have when evaluating the project.

Once constructed, the verification of each system component used physically measured data against the modelled and computer aided simulation results. Problems were encountered but overcome. The final end-to-end system test brought together each component to verify the project was able to produce a controllable sound based on the visible colour information received from the transmitter.

In terms of the project's critical objectives, all were passed.

- Transmit VSL light from user input – PASS
- Detect VSL light from a 50cm communication distance – PASS
- Detect modulated VSL information – PASS
- Create a synthesised tone based on the VSL spectrum – PASS
- Have audible output via powered speakers or mixing desk – PASS
- The system must have audio latency under 10ms – PASS

The end-to-end system test also measured the audio latency to be less than 1ms, thus also fulfilling one of the desirable objectives of decreasing the audio latency to under 5ms. The communication channel distance was 54cm, slightly larger than the minimum 50cm imposed by the critical project objective. The initial results are accepted as passing all critical project objectives, however, there is more work to be done.

8.1 Future Work

In discussing the completion of the project's critical objectives, there is more work that can be done to improve the functionality of the current prototype.

Fundamentally, the areas of interest are the desirable project objectives, however, during the construction and evaluation of the project prototype, several areas of interest could be investigated for possible areas of improvement.

An example of improvement is in the logic translation between the FPGA and the R_x ADC. The current solution was to use a switching transistor and a voltage divider network. Further testing could uncover why the chosen devices did not perform as per the vendor specification. The choice of transistor led to the maximum rate of 2.5MSPS, however, if embedding secondary data in the colour information (as per the desirable project objectives), this rate might be too slow to detect fine resolution changes in phase if using QAM techniques.

Future work could also investigate the NCO algorithm, to investigate why the expected output was not occurring and rectifying the problem. The current unique sound should first be analysed if it could serve as a basis for a local oscillator, with additional NCOs added to produce different characteristics based on the current tones being produced.

Reflecting on Plato's statement, the impact that this project has made as a plausible prototype for a commercial model of a colour based music synthesiser is significant. Using a visual trigger for creating sounds is possible with the technology available today, with the plausible future of seeing artists create music by painting pictures.

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